

Design and Realization of Image Acquisition IP Core Based on Avalon Bus

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Abstract—The present study puts forward a new IP core design for real-time, high-speed image acquisition, based on Avalon bus. The proposed design can be described as follows. First, according to the top-down design philosophy, the IP core was functionally partitioned and hierarchically divided. Second, the IP core was driven and encapsulated under the HAL API. Third, the customized peripheral was added into Nios II system. The following experiment validated the low-power, high real-time of this IP core. Thus the customized image acquisition IP core based on Avalon bus was designed, realized and validated. Since IP core is configurable and can be well transplanted, it can be easily applied to embedded image acquisition system. And the IP core designed above has good portability and universal property.

Index Terms—FPGA, SOPC, Avalon bus, image acquisition, IP core

I. INTRODUCTION

In recent years, with the rapid development of deep sub-micron and ultra-deep sub-micron process engineering, system-level integration (System Level Integration) has become a major hot spots in semiconductor industries, which is a programmable system-on-chip (SOPC), representing the direction of development of electronic design [1]. With the CPLD/FPGA increasing scale, design has become increasingly complex, calling IP core could avoid duplication of effort [2], so the use of IP core is a trend.

With modern electronic technology's rapid development, image acquisition and processing have been increasingly widely used [3]. Image acquisition IP core requests to collect single frame, consecutive frame image data, and enables the user to set the capture window size. Due to the need for follow-up to deal with image compression, image acquisition IP core contains a conversion module of color mode at the same time.

II. HARDWARE LOGIC DESIGN

A. Design Ideas

Image acquisition IP core hardware logic module contains the judgment module of time sequence of images (Cmos Sensor Data Capture), Bayer to RGB module (Bayer Pattern To RGB), RGB to YUV Module (RGB To YUV), Avalon MM slave port module (Avalon

Slave Interface), Avalon MM master port module

(Avalon Master Interface). System structure can be clipped according to the needs.

B. System Block Diagram

Timing judging module (Cmos Sensor Data Capture) can introduce effective data, effective data symbol signal, and the row-column signal into the next module by judging the timing signal of image sensor. Bayer to RGB module (Bayer Pattern To RGB) judges the row-column signal to determine whether to sample, and buffers one-way data as well as transfers Bayer format data to the RGB data, and introduces R, G, B signals into the next module. RGB to YUV Module (RGB To YUV) converts RGB data to YUV data, and introduces the Y, U, V signal to the next module. Avalon MM master port module (Avalon Master Interface) writes Y, U, V data into the cache of double clock FIFO. After read from the double clock FIFO, the Y, U, V data is saved to SDRAM through the Avalon bus [4]. Avalon MM slave module (Avalon Slave Interface) sends control signal and register parameter signal to the Avalon MM master module and other functional modules. System block diagram is shown in Fig. 1.

C. Module Design

Timing of image sensor MT9M011 is shown in Fig. 2 and Fig. 3.

When FRAME_VALID and LINE_VALID signal are both high at the same time, the pixel data are effective. Timing judging module (Cmos Sensor Data Capture) judges the timing signal sent by image sensor and sends the effective image data, effective data sign signal and row-column counting signal into the next module [5]. Using the reverse effective frame signal as the end of a

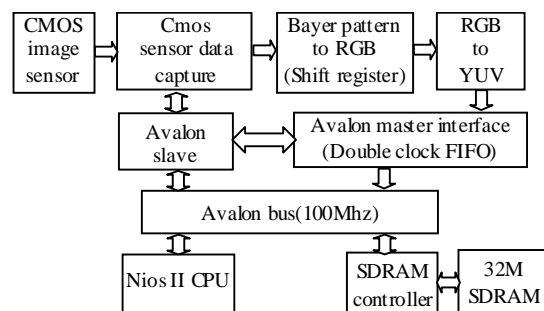


Figure 1. System block diagram.

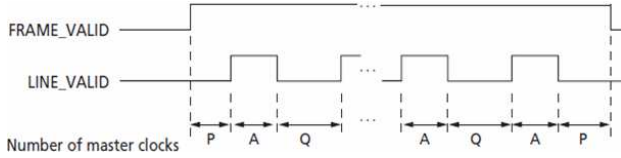


Figure 2. Row synchronization and frame synchronization signal.

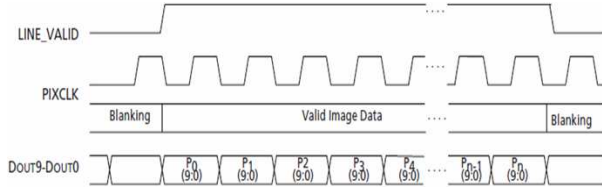


Figure 3. Row synchronization and pixel data.

frame acquisition, the rising edge of this signal will set the first bit of status_register in Avalon MM slave port.

MT9M011 adopts Bayer format. Even row interval include the green and red pixels, and the odd-numbered row interval include the blue and green pixels; even column interval include green and blue pixels, and the odd-numbered column interval include red and green pixels.

This module begin to sample and output new effective sign signal data according to the row-column counting signal sent by the timing judging module. G components are interpolated and then are combined with the R, B cache components into RGB format data.

In this module, we have adopted "RAM based" as the row buffer. The parameter is set as 2-tap, and space as 1280, each tap median as 8 (number_of_taps=2, tap_distance=1280, width=8).

RGB is based on the color space of the three primary colors. And the conversion formula between the color space of brightness and the color space of color difference is:

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B \quad (1)$$

$$U = -0.169 \times R - 0.332 \times G + 0.500 \times B \quad (2)$$

$$V = 0.500 \times R - 0.419 \times G - 0.0813 \times B \quad (3)$$

The multiplication of color components value and decimal coefficient is converted into multiplication of color components value and 8-bit binary number (a corresponded binary number of decimal coefficient multiplied by the 128). The number less than 0 is set as 0, and the number more than 255 is set as 255.

Avalon slave port module maps the internal node into addressable offset address, and Nios II processor read and write through it [6]. Avalon MM slave module sends control signal and register parameter signal to Avalon MM master port, including a variety of interface signal which are in line with the Avalon bus specification [7].

Avalon master port initiates the basic writing transmission and transmits a data unit to the Avalon bus module each time. Avalon MM master port receives control signal and register parameter signal from the Avalon MM slave module including a variety of interface signal which are in line with the Avalon bus specification.

D. Schematic Connection Diagram of Each Module

Linking up the above-mentioned modules together, we get the schematic diagram (Fig. 4). The first from the left is timing judging module, the second from the left is Bayer Pattern To RGB module, the third from the left is RGB To YUV module, the fourth from the left is Avalon MM master port module, and the fifth from the left is Avalon MM slave port module.

III. DEVICE DRIVING AND PACKAGING UNDER HAL

A. Design Ideas

We customized the image acquisition peripherals, so we must provide the device driver and integrate the device driver into the HAL system library. Device driver contains two parts, one part is the head files defining the underlying hardware interface, which is used to describe the device registers and access methods, and the other part is HAL driver files (API function).

B. Register Description

Device driver controls the image acquisition IP core and communicates with the core through the register of memory mapping.

CMOS_GO_BIT 0X01. When CMOS_BUSY_BIT is at high level, CMOS_GO_BIT is set as high level to start a new frame collection.

Status register is composed of many separate status bits which indicate the internal IP core state. Software can read the Status Register at any moment, and will not change its contents. Write 0 to status register will clear all the status bits.

CMOS_FRAME_DONE_BIT 0X01. If the line synchronization signal changes from the high level to low level, CMOS_FRAME_DONE_BIT is set as low level to mark the last frame acquisition has just been completed.

CMOS_BUSY_BIT 0X03. If a new frame data collecting is started, register will set CMOS_BUSY_BIT as high level to mark the collecting core is collecting datas.

CMOS_WRITE_DONE_BIT 0X02. When the count length in the Avalon Master Interface is more than one frame, and the double clock FIFO is empty, register will set CMOS_WRITE_DONE_BIT as high level to mark a completion of one frame image is saved to SDRAM.

Write_address register represents the first input data unit's address in the DMA transmission, that is, the head address of the image collecting data. This 32 bits register can complete addressing for all the slave ports.

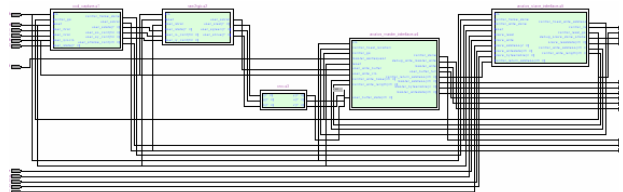


Figure 4. Schematic connection diagram of each module.

C. Software Programming Model

The general type of equipment HAL supported does not match image acquisition IP core, so the user access register through the base address plus address offset manner, thus to control and communicate with the image acquisition IP core [8]. Driver software flow chart is shown in Fig. 5.

Alt_avalon_capture_command (), a subroutine, which is designed to provide common interface access to image acquisition IP core.

Int alt_avalon_capture_command (alt_u32 base, alt_u32 address_reg).

Base is the image acquisition peripheral base address. Address_reg is the head address for data retention. Returned value serve as the current address and can be used as the next frame's head address for data retention.

D. Packaging

Open the SOPC Builder component editor and package the image acquisition logic (Verilog file) into a SOPC Builder element (also known as the IP core) under the GUI (graphical user interface).

Create two new folders under equipment folder: one is inc, where register description file (altera_avalon_cmos_controller_regs.h) is placed; the other one is the HAL, where the device driver files integrated into the HAL system library are placed. Inc folder which under the HAL directory store head file (altera_avalon_cmos_controller.h). Src folder store the altera_avalon_cmos_controller.c file and the device driver Makefile. C file which tends to compile is placed on the C_LIB_SRCS line.

Thus the compiler can find the device driver file, and compile it into the HAL system library. The image acquisition IP core based on the Avalon bus can be used as peripheral components Altera provided.

IV. ANALYSIS OF EXPERIMENTAL RESULTS

The actual experiment was carried out in the Altera's DE2 board, and it used the MICRON's image sensor MT9M011. We connected the main port of image acquisition IP core with SDRAM. After the acquisition was completed, the QVGA image data stored in SDRAM and upload to PC. Adding the head file, the actual image is shown in Fig. 6.

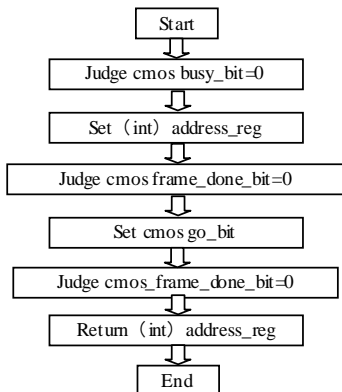


Figure 5. Driver software flow chart.

TABLE I.
RESOURCE CONSUMPTION OF THE IP CORE

Top-level Entity	Coms_burst_write_controller
Family	Cyclone II
Device	EP2C35F672C6
Timing models	Final
Met timing requirements	Yes
Total logic elements	693/33, 216 (2%)
Total combinational functions	592/33, 216 (2%)
Dedicated logic registers	370/33216 (1%)



Figure 6. The effect of the actual image.

V. CONCLUSION

We customized image acquisition peripherals based on the Avalon bus, proposed a SOPC system of image acquisition scheme, and achieved to design a configurable and portable real-time image acquisition IP core. Experimental results reveal that the IP core is in good operation, at a high speed, with good portability and low power consumption, and has a strong practicality and versatility.

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