

# Application of FM24C256 in the Branch Station of Coal Mine Monitoring System

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**Abstract**—FRAM, which has the advantage of ROM and RAM, is the perfect memory in real-time data storage. To solve the problem of mass data storage of Branch Station, the storage architecture grounded on FRAM and CF card is proposed in this paper. It makes full use of the advantage of two different storage technology to solve the problem of mass data storage.

**Index Terms**—fm24c256; data storage; branch station

## I. INTRODUCTION

The branch station of coal mine monitoring system (we call it workstation for short) is the important means to ensure safety production underground, which plays a great role in taking precautions against natural calamities, reducing natural disasters of the mine, and improving productive efficiency. Integrality and varacity of the monitoring data is the crux of coal mine safety production. However, not only the data storage capacity of existing workstations is very limited, but also they are short of efficient data management mechanism. Once there is something wrong, a great deal of data will be lost, which may bring about dangers to safety production.

By analyzing the technology of storage and data management strategy, the storage architecture grounded on CF card and FRAM is proposed to use in advanced workstation. It makes full use of the advantage of different storage technology to solve the problem of mass data storage. The CompactFlash Memory Card supports three operational modes: (1) PC card ATA using I/O mode, (2) PC card ATA using Memory mode, and (3) TrueIDE mode [1][2]. The hardware design, driver design and control software design in TrueIDE mode are discussed, for more detail information, please reference the additional paper, namely Application of CompactFlash Card in the Branch Station of Coal Mine Monitoring System [3].

FRAM, which has the advantage of ROM and RAM, is the ideal memory for non-volatile memory applications requiring frequent or rapid writes or low power operation [4]. In workstation, monitoring information is firstly stored in FRAM, and then stored in CF card when it achieves certain quantity, which makes full use of the advantage of different storage technology to solve the problem of mass data storage.

This paper mainly introduces the design and implementation of FRAM in the Branch Station of Coal Mine Monitoring System letter for each word.

## II. GENERAL DESCRIPTION OF FM24C256

The FM24C256 devices are 256 Kbits CMOS nonvolatile electrically erasable memory. These devices offer the designer different low voltage and low power options. They conform to all requirements in the Extended IIC 2-wire protocol. Furthermore, they are designed to minimize device pin count and simplify PC board layout requirements. The entire memory array can be write disabled (Write Protection) by connecting the WP pin to VCC. Functional address lines allow up to eight devices on the same bus, for up to a total of 2 Mbit address space. The IIC communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption. The block diagram of FM24C256 is shown in Figure 1.

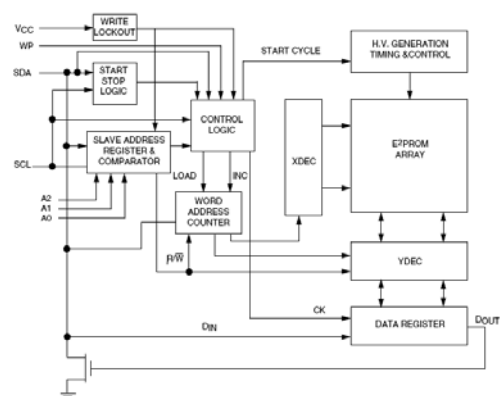


Figure 1. the block diagram of FM24C256

The IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition. In addition, since the IIC bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or control byte, must follow the START condition. For EEPROMs, the first 4-bit of the control byte is 1010 binary for READ

and WRITE operations. This is then followed by the device selection bits A2, A1 and A0, and acts as the three most significant bits of the word address. The final bit in the control byte determines the type of operation performed (READ/WRITE). A "1" signifies a READ while a "0" signifies a WRITE. The control byte is then followed by two bytes that define the word address, which is then followed by the data byte. The EEPROMs on the IIC bus may be configured in any manner required, providing the total memory addressed does not exceed 512K bits (64K bytes). EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. All unused pin must be tied to VSS.

### III. HARDWARE DESIGN OF FM24C256

The following hardware design description refers to the detailed schematic diagram Figure 2.

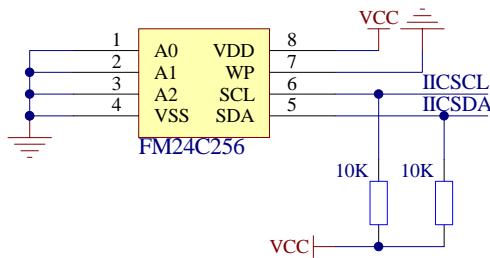


Figure 2. Circuit between FM24C256 and LPC2210

The FM24C256 employs a bi-directional two-wire bus protocol using few pins and little board space. Figure 3 illustrates a typical system configuration using the FM24C256 in a microcontroller-based system. A0-A2 are used to select one of up to 8 devices of the same type on the same two-wire bus. To select the device, the address value on the three pins must match the corresponding bits contained in the device address. When WP is high, the entire array will be write-protected. When WP is low, all addresses may be written. SDA is used to shift serial data and addresses for the two-wire interface. The input buffer incorporates a Schmitt trigger for improved noise immunity and the output driver has slope control for falling edges. SCL is the serial clock input for the two-wire interface. Data is clocked out of the device on the SCL falling edge, and clocked in on the SCL rising edge. The SCL input also incorporates a Schmitt trigger input for improved noise immunity.

### IV. SOFTWARE DESIGN

The FM24C256 is a serial FRAM memory. The memory array is logically organized as 32,768 x 8 bit memory array and is accessed using an industry standard two-wire interface.

When accessing the FM24C256, the user addresses 32,768 locations each with 8 data bits. These data bits are shifted serially. The 32,768 addresses are accessed using the two-wire protocol, which includes a slave address to distinguish from other non-memory devices, and an extended 16-bit address. Only the lower 15 bits are used by the decoder for accessing the memory. The upper

address bit should be set to 0 for compatibility with higher density devices in the future. The complete operation of writes is explained below.

All writes begin with a device address, then a memory address. The bus master indicates a write operation by setting the LSB of the device address to a 0. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h. The flow chart of writing data to FM24c256 is showed in Figure 3.

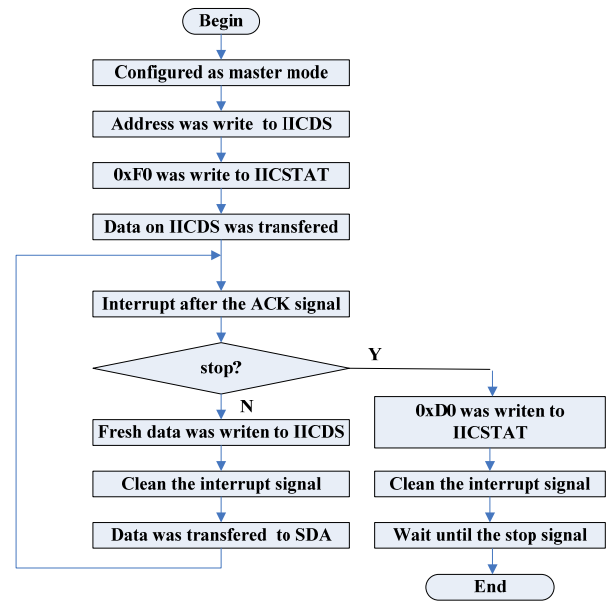


Figure 3. the flow chart of writing data to FM24C256

Unlike other nonvolatile memory technologies, there is essentially no write delay with FRAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay on the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including a read or write can occur immediately following a write command. Acknowledge polling, a technique used with EEPROM to determine if a write has completed is unnecessary and will always return a ready condition. Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the Acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using a Start or Stop condition prior to the 8th data bit. The FM24C256 uses no page buffering. The memory array can be write protected using the WP pin. Pulling the WP pin high will write-protect all addresses. The FM24C256 will not acknowledge data bytes that are written when WP is active. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP low will deactivate this feature. WP is internally pulled down. The state of WP should

remain stable from the Start command until the address is complete.

#### ACKNOWLEDGMENT

This work is supported by Zhejiang province fatal project (priority subjects) key industrial project (2008C11011)

#### CONCLUSION

By analyzing the technology of storage and data management strategy, the storage architecture grounded on CF card and FRAM is proposed to use in workstation. which makes full use of the advantage of different storage technology to solve the problem of mass data storage, ensures the compatibility of data format between

workstation and personal computer. and makes it convenient in data analysis and processing.

#### REFERENCES

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