

# Comparative Study on Leakage Current of Power-Gated SRAMs for 65-nm, 45-nm, and 32-nm Technology Nodes

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**Abstract**— In this paper, we compare four SRAM circuits. They are the conventional SRAM1, the SRAM2 with power switches on  $V_{SS}$  line, the SRAM3 with switches on  $V_{DD}$  line, and the SRAM4 with switches on both  $V_{DD}$  and  $V_{SS}$  lines, respectively. Among the four SRAMs, the SRAM2 shows the smallest amount of leakage, because its subthreshold leakage is most suppressed by its BODY and Drain-Induced Barrier Lowering (DIBL) effects. In addition, the area overheads of the SRAM2, SRAM3, and SRAM4 are also compared thus the SRAM2 being found most favorable in terms of the area penalty. To reduce the oxide-tunneling leakage more, the SRAM5 with precharge voltage lowering is considered in this paper. Compared with the SRAM2 without lowering the precharge voltage, amounts of leakage of the SRAM5 are suppressed by 24.4%, 13.1%, and 4.2%, respectively, at  $-25^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , and  $100^{\circ}\text{C}$ , for the 65-nm node.

**Index Terms**— Oxide-tunneling leakage, Sub-threshold leakage, Low-leakage, SRAM, Memory

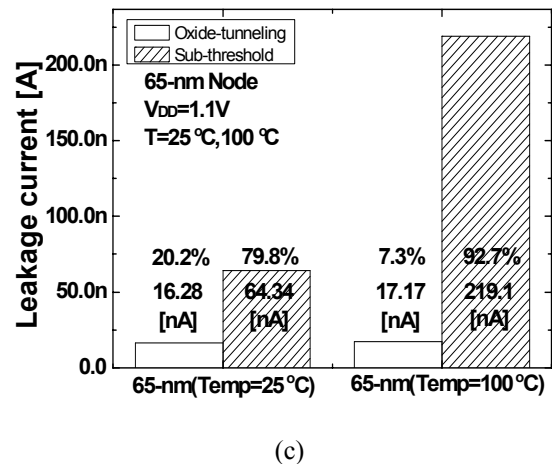
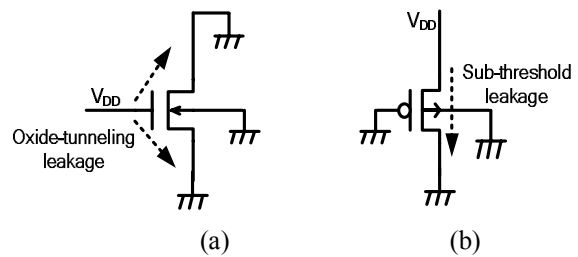
## I. INTRODUCTION

As channel length goes shorter than 70 nm, a leakage component in power dissipation is emerging to compete with the switching one [1]. Though many techniques have been proposed to suppress leakage current since 1990s, most of them aimed at logic circuits. This is not the right way in sub-70-nm era, because embedded memories such as SRAMs take a larger portion of chip area than logic circuits as times go on [2]. Low-leakage techniques for memory circuits are getting more important recently.

Though a subthreshold component in leakage current has been traditionally considered as a main source of leakage current, the other known by an oxide-tunneling component becomes larger, too, as the gate oxide becomes thinner than before. Thus the oxide-tunneling component in leakage can no longer be ignored in estimating the total leakage current of a chip. Figures 1(a) and (b) describe the current paths for oxide-tunneling leakage and subthreshold leakage, respectively. Figures 1(c) and (d) compare the sub-threshold and oxide-tunneling components in leakage at  $25^{\circ}\text{C}$  and  $100^{\circ}\text{C}$ , respectively. The Spice parameters are obtained from the latest Predictive Technology Models (PTMs) for the technology nodes of 65-nm and 32-nm [3]. In the 65-nm PTM with  $25^{\circ}\text{C}$ , its oxide-tunneling and subthreshold

components take 20.2% and 79.8% of the total leakage current, respectively, in Figure 1(c). When the temperature is up to  $100^{\circ}\text{C}$ , the subthreshold component in leakage becomes as large as 92.7%, while the tunneling one falls to as small as only 7.3%.

Comparison between the tunneling and subthreshold components in leakage of the 32-nm node is also done in Figure 1(d). At  $25^{\circ}\text{C}$ , the subthreshold and tunneling components for the 32-nm are 95.2% and 4.8%, respectively, compared with 79.8% and 20.2% of the 65-nm. Similarly, at  $100^{\circ}\text{C}$ , the subthreshold and tunneling components are 98.2% and 1.7% for the 32-nm, respectively, compared with 92.7% and 7.3% for the 65-nm. This is because reduction of the oxide leakage due to lowering the supply voltages is more dominant than increase in leakage due to the gate oxide thinning in the 32-nm node.



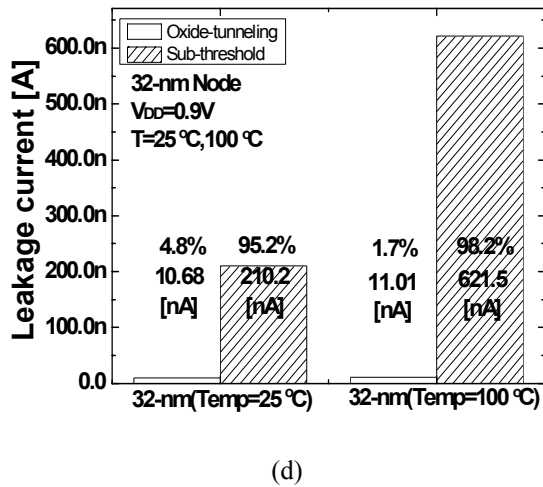


Figure 1. (a) A current path for the oxide-tunneling leakage (b) A current path for the subthreshold leakage (c) Comparison of the tunneling and subthreshold components in leakage with the 65-nm Predictive Technology Model at 25°C and 100°C (d) Comparison of the tunneling and subthreshold components in leakage with the 32-nm Predictive Technology Model at 25°C and 100°C

Leakage suppression techniques can be divided into two groups. One is using the body-bias control [4] and the other is inserting power switches on power lines [5], [6], [7], [8]. If only oxide-tunneling leakage is a concern, the body-bias control can not be a solution, because the oxide-tunneling leakage can not be improved by controlling body-bias voltages. On the contrary, inserting the power switches between the source lines of SRAM cell array and the power lines can control the source-line voltages dynamically resulting in suppressing both subthreshold and oxide-tunneling leakage.

There can be three methods of inserting the power switches on the power lines. The first one is inserting an NMOSFET switch on the  $V_{SS}$  power line. Here the  $V_{SS}$  and  $V_{DD}$  are the power lines of ground and supply voltage, respectively. The second one is inserting a PMOSFET switch on the  $V_{DD}$  power line. The third one is inserting both NMOSFET and PMOSFET switches on both the  $V_{SS}$  and  $V_{DD}$  lines, respectively. All of them are effective in suppressing subthreshold leakage. Their impacts on oxide-tunneling leakage, however, have not been investigated well.

In this paper, the three methods mentioned just earlier are compared to find which one is most favorable in terms of suppressing both the oxide-tunneling and subthreshold leakage in the 65-nm and 45-nm nodes [9]. In addition, the comparison is extended to the future 32-nm node in this paper and the area overheads between the SRAMs with different power gating switches are also discussed in the later section. To reduce oxide-tunneling leakage more, an SRAM circuit with precharge voltage lowering is investigated to know how much it can save the leakage for the 65-nm, 45-nm and 32-nm nodes in the section IV and finally we make conclusions in the section V.

## II. SRAM CIRCUITS WITH POWER GATING

Figure 2 shows a schematic of the SRAM1 which represents the conventional SRAM. Here the MN1, MN2, MP1, and MP2 form a cross-coupled inverter latch and the MN3 and MN4 are word-line inverters through which the bit lines are connected to the latch. In Figure 2, if the Q and QB nodes have high and low, respectively, subthreshold leakage flows through the MP2 and MN1. This leakage through the MP2 and MN1 is called by the cell leakage. In addition, there is the other leakage current through the MN4 from the BLB node to the  $V_{SS}$ . Here, because both the Q and BL nodes have high, subthreshold leakage does not flow through the MN3. The leakage of the MN4 is called by the bit-line leakage. Both the cell and bit-line leakage currents belong to the subthreshold component of leakage dissipation. The oxide-tunneling component of leakage can flow through all the transistors as shown in Figure 2. Their leakage paths are indicated by the dotted arrows in Figure 2.

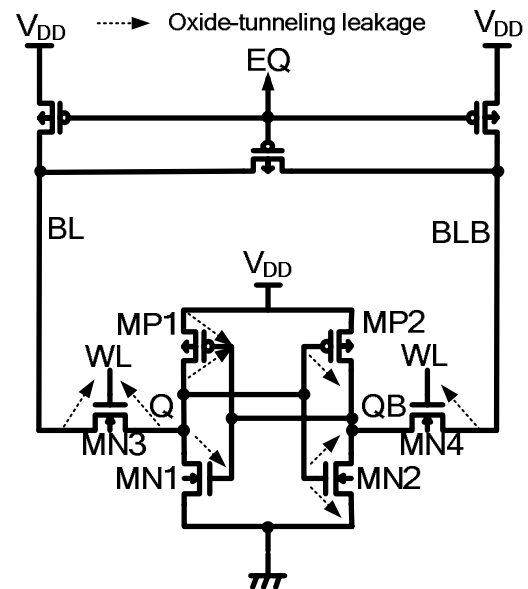


Figure 2. SRAM1 circuit which is the conventional

Figure 3 shows a schematic of the SRAM2, where the MN5 is inserted between the source line of the MN1 and MN2 and the  $V_{SS}$  power line. Both the MN6 and MN7 have the diode-connected configuration as shown in Figure 3. When the MN5 is turned off, the source-line voltage of the MN1 and MN2 represented as the  $V_{SL}$  is increased from  $V_{SS}$  to  $2V_{TH}$  by the MN6 and MN7, thus lowering a retention voltage of the cell by  $2V_{TH}$ . Here  $V_{TH}$  means threshold voltage. Because the BODY and Drain-Induced Barrier Lowering (DIBL) effects become stronger as the  $V_{SL}$  increases higher, the subthreshold component of leakage can be reduced when the retention voltage is lowered. And, because voltages across the oxides of the SRAM2 decrease with lowering the retention voltage, their oxide-tunneling leakage currents become smaller with increasing the  $V_{SL}$ , too.

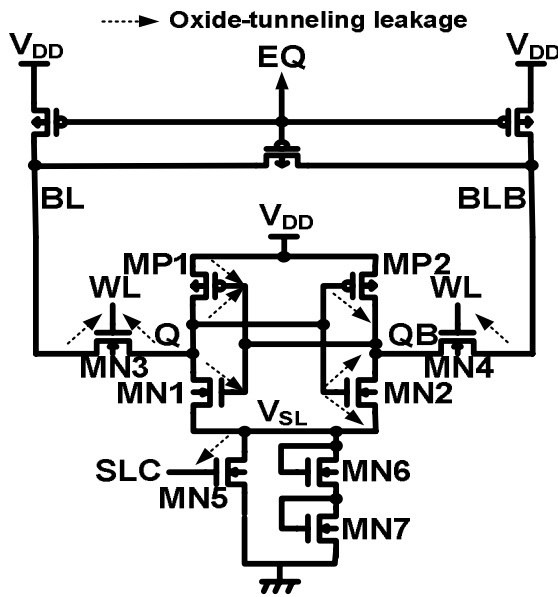


Figure 3. SRAM2 circuit with its power switch on the VSS line

Figure 4 shows a schematic of the SRAM3, where the MP3 is inserted between the source-line of the MP1 and MP2 and the  $V_{DD}$  line. In Figure 4, when the MP3 is turned off, the source-line voltage of the MP1 and MP2 represented as the  $V_{SH}$  drops by  $2V_{TH}$  through the MN5 and MN6. Thus the retention voltage is reduced from  $V_{DD}$  to  $V_{DD}-2V_{TH}$ . Like the SRAM2, the BODY and DIBL effects get stronger as the  $V_{SH}$  decreases lower. This helps its subthreshold leakage be decreased more. Like Figure 3, because voltages across the oxides of the transistors in Figure 4 are decreased, their oxide-tunneling leakage currents are reduced, too.

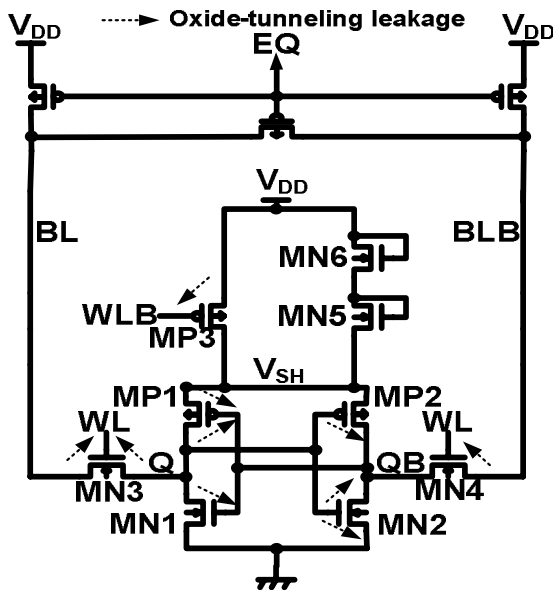


Figure 4. SRAM3 circuit with its power switch on the  $V_{DD}$  line

Figure 5 shows a schematic of the SRAM4 which seems like a combination of the SRAM2 and SRAM3. Here, the MN5 and MP3 are inserted between the  $V_{SL}$  and  $V_{SS}$  and between the  $V_{DD}$  and  $V_{SH}$ , respectively. The MN6 and MP4 are diode-connected MOSFETs. When the MN5 and MP3 are turned off, its retention voltage defined by voltage difference between the  $V_{SL}$  and the  $V_{SH}$  is reduced from  $V_{DD}$  to  $V_{DD}-2V_{TH}$ .

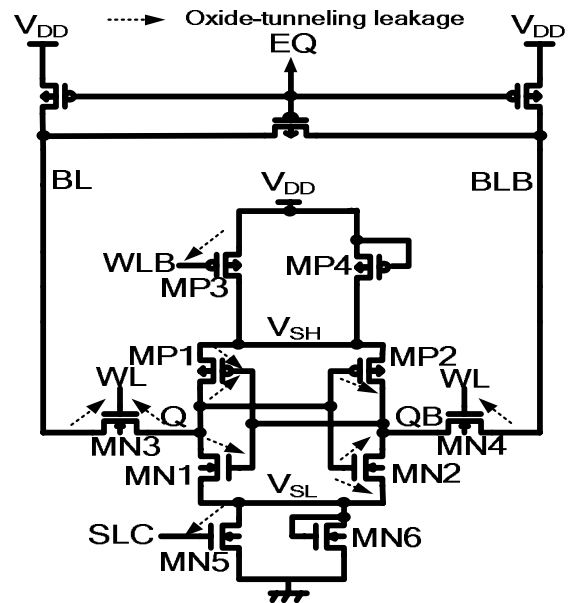


Figure 5. SRAM4 circuit with its power switches on both the  $V_{SS}$  and  $V_{DD}$  lines

### III. LEAKAGE COMPARISON

Table 1 summarizes the leakage dissipation of the four SRAMs shown in Figures 2, 3, 4, and 5, respectively, with the 65-nm PTM [3]. To analyze their leakage dissipation, the oxide-tunneling and subthreshold components are simulated here, respectively. The temperatures are  $-25^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , and  $100^{\circ}\text{C}$ .

TABLE I.

LEAKAGE CURRENTS OF THE FOUR SRAMs WITH THE 65-NM PTM AT  $-25^{\circ}\text{C}$ ,  $25^{\circ}\text{C}$ , AND  $100^{\circ}\text{C}$

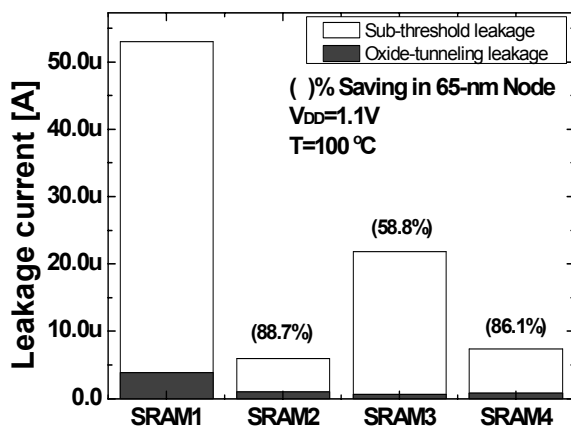
65-nm Node $V_{DD}=1.1\text{V}$	Temperature	Total leakage	Oxide-tunneling leakage	Sub-threshold leakage	Cell retention Voltage
		[ $\mu\text{A}$ ]	[ $\mu\text{A}$ ]	[ $\mu\text{A}$ ]	[V]
SRAM1	T= $-25^{\circ}\text{C}$	7.95	3.62	4.33	1.1
	T= $25^{\circ}\text{C}$	18.15	3.7	14.45	1.1
	T= $100^{\circ}\text{C}$	53.07	3.83	49.24	1.1
SRAM2	T= $-25^{\circ}\text{C}$	1.23	0.97	0.26	0.77
	T= $25^{\circ}\text{C}$	2.14	1.02	1.12	0.78
	T= $100^{\circ}\text{C}$	5.96	1.03	4.93	0.78
SRAM3	T= $-25^{\circ}\text{C}$	2.25	0.7	1.55	0.73
	T= $25^{\circ}\text{C}$	6.42	0.67	5.75	0.71
	T= $100^{\circ}\text{C}$	21.87	0.59	21.28	0.66
SRAM4	T= $-25^{\circ}\text{C}$	1.21	0.89	0.32	0.78
	T= $25^{\circ}\text{C}$	2.4	0.89	1.51	0.78
	T= $100^{\circ}\text{C}$	7.37	0.83	6.54	0.75

Of the four SRAMs, the SRAM3 has the smallest amounts of oxide-tunneling leakage for all temperatures. This is because the MN3 and MN4 in Figure 4 suffer

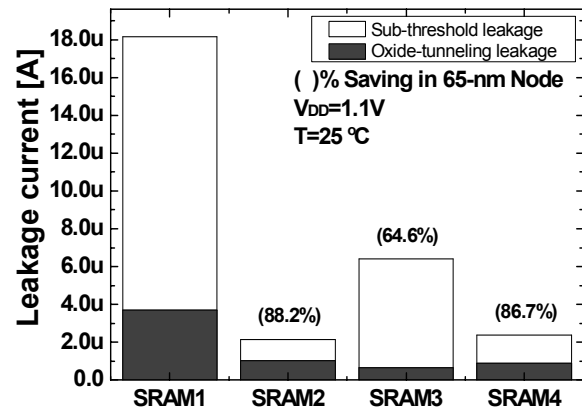
lower stress across their oxides than the others when the MP3 is turned off. Despite this small tunneling leakage, its subthreshold component seems to be suppressed very less than the SRAM2 and SRAM4. This is caused from the channel width of the MP1 and MP2 is only a third of the MN1 and MN2 generally. Though the BODY and DIBL effects of the MP1 and MP2 decrease the subthreshold current through the MP1 and MP2 with the  $V_{SH}$  decreasing, they hardly impact on the the total subthreshold leakage of the SRAM3. The MN1 and MN2 which dominate the total subthreshold current of the SRAM3 do not have the BODY effect thus their subthreshold leakage not being able to decrease.

Comparing leakage dissipation of the SRAM2 and SRAM4, the total leakage of the SRAM2 seems smaller than the SRAM4 at 25°C and 100°C, whereas slightly larger at the temperature as low as -25°C. It is well known that the subthreshold leakage has a temperature dependence much stronger than the oxide-tunneling leakage thus a portion of the oxide-tunneling component in leakage increasing with the temperature going down. On the contrary, the subthreshold leakage becomes more dominant at higher temperatures. Hence, at -25°C, because the tunneling leakage of the SRAM4 is smaller than the SRAM2, its total leakage becomes smaller than the SRAM2, too. At higher temperatures such as 25°C and 100°C, however, the total leakage of the SRAM2 becomes smaller than the SRAM4. This is caused from the SRAM2 has the BODY effect on the MN1 and MN2 stronger than the SRAM4. Because the MN1 and MN2 are wider than the other transistors, suppressing leakage of the MN1 and MN2 gives the largest impact on lowering the total leakage dissipation of the SRAM2.

Figures 6(a) and (b) compare the leakage of the four SRAMs when the temperatures are 100°C, and 25°C, respectively, by using the 65-nm PTM. Comparing the SRAM2 with the conventional SRAM1, 88.7% of its leakage is saved, while the percentage saving of the SRAM3 is only as small as 58.8% and that of the SRAM4 is 86.1%. When the temperature is 25°C, the percentage saving of the SRAM2 is 88.2%.



(a)



(b)

Figure 6. Leakage comparison of the four SRAMs with the 65-nm PTM (a) at 100°C and (b) at 25°C

Table 2 compares the leakage dissipation of the four SRAMs with the 45-nm PTM [3]. Like Table 1, the temperatures are kept at -25°C, 25°C, and 100°C. Comparing the leakage dissipation of the four SRAMs, the SRAM2 shows the lowest dissipation of leakage among them. This result is the same with Table 1. And, comparing the 45-nm and 65-nm PTMs indicates amounts of the percentage saving of leakage of the SRAM2 with the 45-nm PTM seem better than those with the 65-nm.

Figures 7(a) and (b) compare the leakage of the four SRAMs when the temperatures are 100°C and 25°C, respectively, by using the 45-nm PTM. In Figure 7(a) at the 100°C with the 45-nm PTM, the SRAM2, SRAM3, and SRAM4 can save their leakage currents as large as 92%, 64.6%, and 90.1% of the leakage of the SRAM1, respectively. Among the SRAM2, SRAM3, and SRAM4, the SRAM2 saves the largest amount of leakage than the other two because its subthreshold leakage is decreased most. Concerning the oxide-tunneling leakage, however, the SRAM4 has smaller values than the SRAM2, though the total leakage of the SRAM2 is smaller than the SRAM4. For the temperature of 25°C which is shown in Figure 7(b), the results are almost similar with the 100°C of Figure 7(a). Only to comment here is that leakage saving of the SRAM2 is larger than that of the SRAM4 only by 1.2% at 25°C whereas the difference is 1.9% at 100°C. As the temperature becomes lower, the subthreshold leakage currents of both the SRAM2 and SRAM4 decrease thus difference in savings between them becoming smaller, too.

TABLE II.

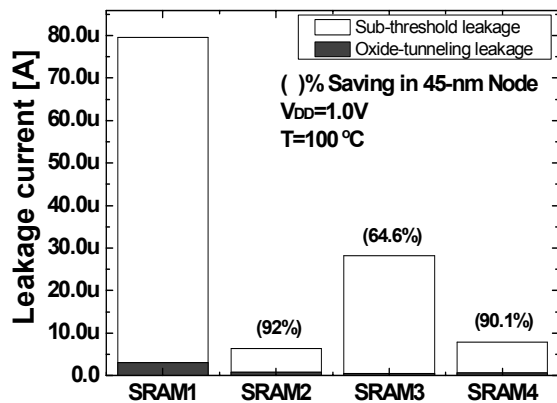
LEAKAGE CURRENTS OF THE FOUR SRAMs WITH THE 45-NM PTM AT -25°C, 25°C, AND 100°C

45-nm Node V <sub>DD</sub> =1.0V		Total leakage [uA]	Oxide-tunneling leakage [uA]	Sub-threshold leakage [uA]	Cell retention Voltage [V]
SRAM1	T=-25	10.61	3.01	7.6	1
	T=25	26.9	3.06	23.84	1
	T=100	79.6	3.14	76.46	1
SRAM2	T=-25	1.1	0.82	0.28	0.67
	T=25	2.08	0.84	1.24	0.68
	T=100	6.35	0.84	5.51	0.67
SRAM3	T=-25	2.87	0.57	2.3	0.62
	T=25	8.49	0.53	7.96	0.59
	T=100	28.15	0.47	27.68	0.55
SRAM4	T=-25	1.1	0.72	0.38	0.67
	T=25	2.41	0.71	1.7	0.67
	T=100	7.85	0.65	7.2	0.64

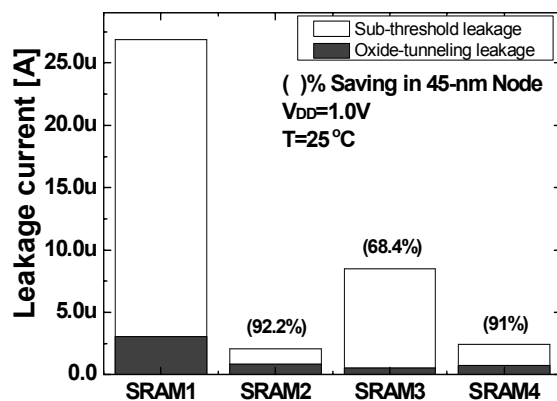
Table 3 is for the leakage dissipation of the 4 SRAMs with the 32-nm PTM [3]. Here the temperatures are kept at -25°C, 25°C, and 100°C. Comparing the leakage dissipation of the four SRAMs, the SRAM2 shows the lowest dissipation of leakage among them as it does in Tables 1 and 2. And, comparing the 65-nm, 45-nm, and 32-nm PTMs indicates the percentage saving of leakage of the SRAM2 with the 32-nm PTM seems largest among the three 65-nm, 45-nm, and 32-nm PTMs. As the technology node becomes smaller, for example, from 65-nm via 45-nm toward 32-nm, the subthreshold leakage current increases sharply due to its lower threshold voltage according to the device scaling trend. For the oxide-tunneling leakage, however, the increase in leakage with device scaling looks much more smaller than the subthreshold. This is attributed to the supply voltage lowering compensating the effect of oxide thinning. Hence, the 32-nm node where the subthreshold component takes the largest portion in the total leakage can save the largest amount of leakage among the three nodes.

Figures 8(a) and (b) compare the leakage of the four SRAMs when the temperatures are 100°C and 25°C, respectively, by using the 32-nm PTM. In Figure 8(a), saving in leakage of the SRAM4 is 93.7% and for the SRAM2, the saving reaches 94.6% at 100°C and V<sub>DD</sub>=0.9V. In Figure 8(b) at 25°C and the same V<sub>DD</sub>, amounts of the saving of the SRAM4 and the SRAM2 are 94.7% and 95.5%, respectively. Mentioning the real numbers in Table 3, the leakage of the SRAM2 is only as low as 7.699uA but that of the conventional SRAM1 is as large as 143.6uA at 100°C, thus the SRAM2 saving 94.6% of the leakage power dissipation than the SRAM1.

Table 4 compares the area overheads of the four SRAMs. The overheads of the SRAM2 and SRAM3 are the same because the added power switch of the SRAM2 takes the same area with that of the SRAM3. The SRAM4 having both the NMOSFET and PMOSFET switches needs a larger area than the SRAM2 and SRAM3. Here the area comparison is done by using 0.25-um design rule from industry, because it is difficult to access sub-70-nm design rules. And, in this comparison, it is assumed that four memory cells neighboring share one power switch. For the SRAM4, however, the MN5 and MP3 make up one set of power switches that are shared by four neighboring cells. This assumption of the four cells sharing one power switch is based on the results from the reference [6] which addresses that the read delay penalty degrades with increasing the number of the cells sharing one power switch. If eight cells share one power switch, the read delay penalty exceeds an acceptable limit in spite of the area penalty being improved very much. Finally, it should be noted that the diode-connected MOSFETs of the SRAM2, SRAM3, and SRAM4 take very small areas enough to be neglected. They do not need to be inserted cell by cell or by every four cells like the power switch. Instead, they can be put on the power lines row by row. One row needs only one set of diode-connected switches regardless of how many cells belonging to one row, because the functions of the diode-connected switches are to maintain the retention



(a)



(b)

Figure 7. Leakage comparison of the four SRAMs with the 45-nm PTM at (a) 100°C and (b) 25°C

voltages of the SRAM2, SRAM3, and SRAM4 when the row is not activated.

TABLE III.

LEAKAGE CURRENTS OF THE FOUR SRAMS WITH THE 32-nm PTM AT -25°C, 25°C, AND 100°C

32-nm Node V <sub>DD</sub> =0.9V		Total leakage [uA]	Oxide-tunneling leakage [uA]	Sub-threshold leakage [uA]	Cell retention Voltage [V]
SRAM1	T=-25 °C	20.78	2.59	18.19	0.9
	T=25 °C	52.48	2.63	49.85	0.9
	T=100 °C	143.6	2.67	140.93	0.9
SRAM2	T=-25 °C	1.133	0.721	0.41	0.57
	T=25 °C	2.385	0.727	1.66	0.57
	T=100 °C	7.699	0.716	6.98	0.56
SRAM3	T=-25 °C	4.94	0.476	4.46	0.51
	T=25 °C	13.99	0.446	13.5	0.48
	T=100 °C	41.71	0.402	41.3	0.44
SRAM4	T=-25 °C	1.15	0.605	0.55	0.57
	T=25 °C	2.73	0.581	2.15	0.55
	T=100 °C	8.99	0.533	8.46	0.53

TABLE IV.

AREA OVERHEADS OF THE FOUR SRAMS

Area Overhead [%]	SRAM1	SRAM2	SRAM3	SRAM4
	100	109.2	109.2	123.6

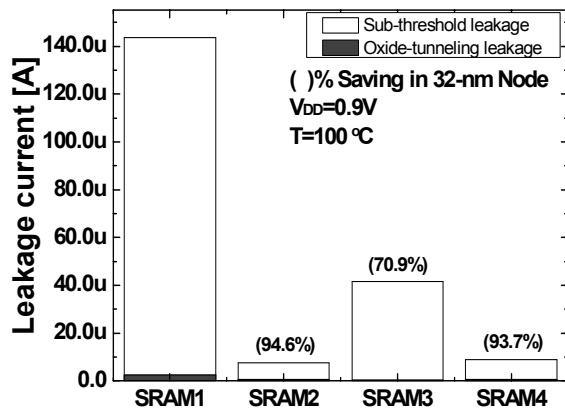
IV. PRECHARGE VOLTAGE LOWERING TO REDUCE THE OXIDE-TUNNELING LEAKAGE

From the leakage comparison among the four SRAMs in the previous sections, the SRAM2 is found to consume the smallest amount of leakage among them. From Tables 1, 2, and 3, we can know that the SRAM2 has tunneling leakage larger than the SRAM4, though its total leakage is smaller. This is because the MN3 and MN4 of the SRAM2 feel the oxide stress higher than the SRAM4 thus the SRAM2 having larger tunneling leakage. To decrease this high oxide stress of the MN3 and MN4 of the SRAM2 and finally to reduce the tunneling leakage of the SRAM2 more, its precharge voltage has to be lowered. Figure 9 shows a schematic of the SRAM5, where its precharge voltage is lowered by using the diode-connected NMOSFETs to reduce the oxide stress of the MN3 and MN4 of the SRAM5.

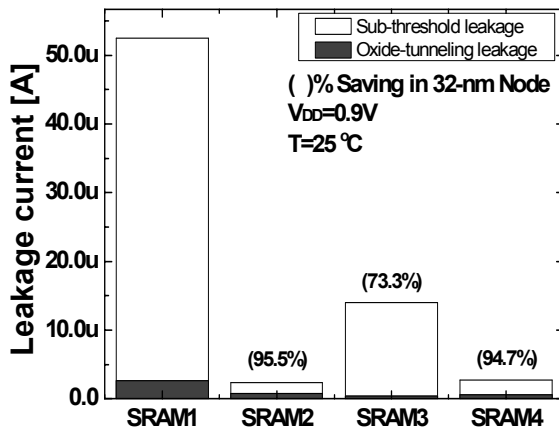
Figures 10(a) and (b) compare oxide-tunneling leakage between the SRAM2 and SRAM5 at 100°C and 25°C, respectively. The simulation is done by using the 65-nm PTM and V<sub>DD</sub>=1.1V. First of all, it is seen that the leakage through the MN3 is larger than the MN4 for both the SRAM2 and SRAM5. This comes from the assumption that the Q and QB nodes are high and low, respectively. When the WL node in Figure 9 is low, tunneling leakage occurs at both the source and drain of the MN3 but for the MN4 only the drain has the leakage. And, tunneling leakage through the cell is the same between the SRAM2 and SRAM5.

For the total tunneling current, lowering the precharge voltage (V<sub>PRE</sub>) only by 0.2V improves the total leakage as much as 24.2% as indicated in Figure 10(a), when the temperature is 100°C. Further detailed analysis is also given in Figure 10(a), where the MN3 of the SRAM5 saves 31.3% more than the SRAM2 and the MN4 does 62.3%. Here the Q and QB nodes are assumed high and low, respectively. In this case, the MN4 saves a larger percentage of leakage than the MN3 because the leakage between the gate of the MN3 and the Q node can not be decreased in spite of lowering the precharge voltage. For the MN4, a tunneling leakage path is found only through between the gate and the BLB and a voltage across the path is lowered by reducing the precharge voltage thus the tunneling leakage decreasing.

In Figure 10(b) with 25°C, the MN3 of the SRAM5 saves more tunneling leakage than the SRAM2 by 35.8% and the MN4 does by 71.3%. The total oxide-tunneling leakage is saved by 27.4% at 25°C. Percentage saving at 25°C is larger than 100°C. This is because a tunneling component of leakage takes a larger portion in total



(a)



(b)

Figure 8. Leakage comparison of the four SRAMs with the 32-nm TM at (a) 100°C and (b) 25°C

leakage as temperature goes down. At the lower temperatures, the larger percentage saving can be achieved as indicated from the comparison between Figures 10(a) and (b).

Figures 11(a) and (b) also compare oxide tunneling leakage between the SRAM2 and SRAM5 with the 45-nm PTM and  $V_{DD}=1V$ , at 25°C and 100°C, respectively. The results show the same trends with Figures 10(a) and (b). In Figure 11(a) with 100°C, the MN3 and MN4 of the SRAM5 save their tunneling leakage more than the SRAM2 by 29% and 57.3%, respectively. Totally, the SRAM5 saves 23.8% more than the SRAM2 by lowering its precharge voltage. Similarly, in Figure 11(b) with 100°C, the MN3 and MN4 of the SRAM5 save more than the SRAM2 by 34.4% and 68%, respectively, and saving in the total tunneling leakage of the SRAM5 reaches 28.5%. This value obtained at 25°C is a little larger than 100°C, because a percentage tunneling component at lower temperature is larger than at higher.

Figures 12(a) and (b) are for the 32-nm PTM with  $V_{DD}=0.9V$ . Amounts of percentage saving in tunneling leakage of the 32-nm at 100°C and 25°C are 24.7% and 29.4%, respectively, when the SRAM5 is compared with the SRAM2.

Figure 13(a) compares the leakage including both oxide-tunneling and subthreshold components between the SRAM2 and SRAM5 at three temperatures of 100°C, 25°C, and -25°C. The 65-nm PTM and  $V_{DD}=1.1V$  are used. At 100°C, percentage saving of the leakage of the SRAM5 is 4.2%. At 25°C and -25°C, amounts of the percentage saving increase to 13.1% and 24.4%, respectively. Figure 13(b) is obtained with the 45-nm PTM and  $V_{DD}=1.0V$ . In Figure 13(b), saving of the SRAM5 is only 3.2% at 100°C but these values become 11.5% and 23.6%, respectively, at 25°C and -25°C. Figure 13(c) is for the 32-nm PTM and  $V_{DD}=0.9V$ . Similarly, percentage saving in Figure 13(c) begins from 2.4% at 100°C. As temperature goes down to 25°C, the saving rises up to 9.1% and at -25°C, finally to 20.8%. Comparing the 65-nm, 45-nm, and 32-nm nodes, it can be seen that the 32-nm saves the least percentage and the 65-nm does the most. This means that the precharge voltage lowering which impacts on lowering only oxide-tunneling leakage is more effective in the 65-nm where the percentage tunneling component in leakage is larger than the 45-nm and 32-nm as stated earlier.

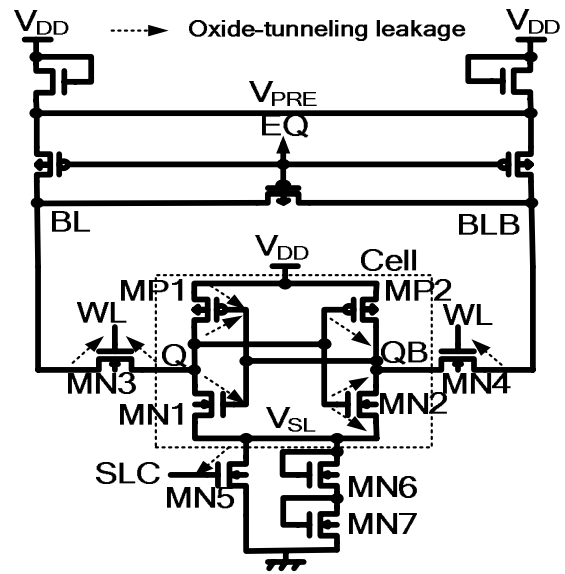
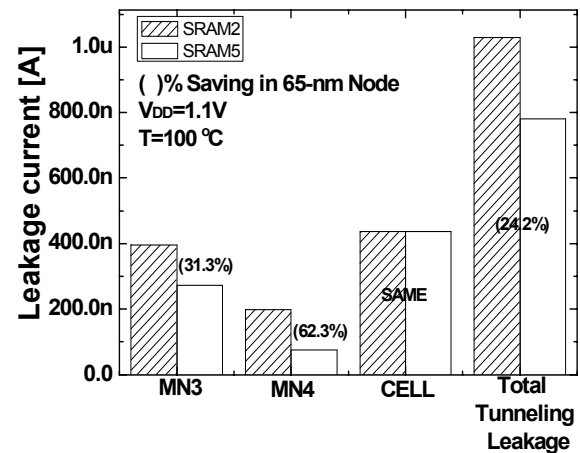
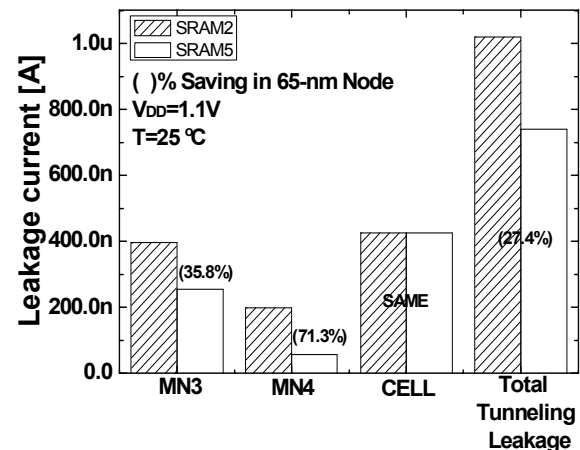


Figure 9. SRAM5 circuit with lowering of its precharge voltage

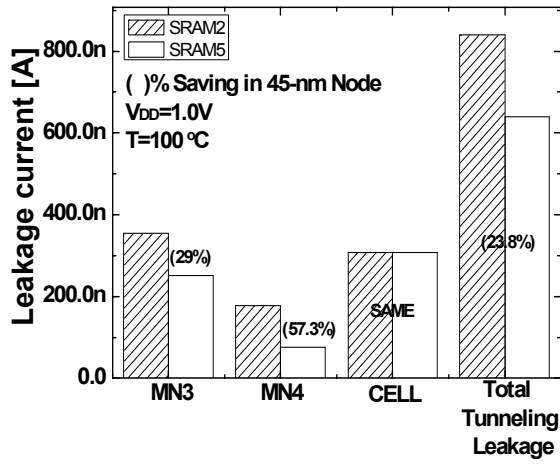


(a)

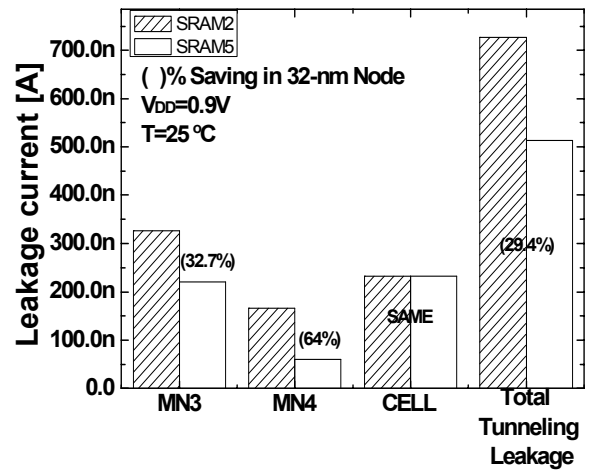


(b)

Figure 10. Oxide-tunneling leakage of the MN3, MN4 and the cell of the SRAM5 with the 65-nm PTM at (a) 100°C and (b) 25 °C

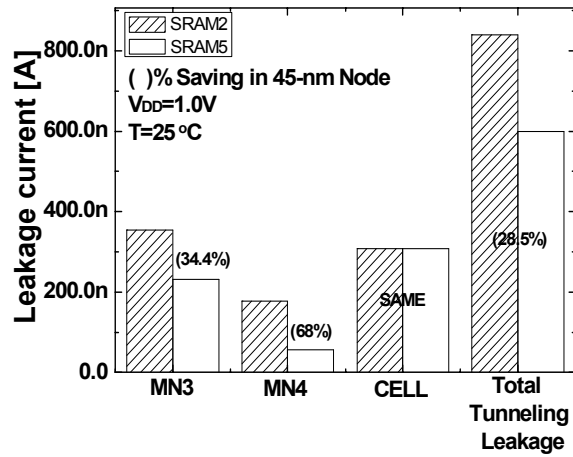


(a)

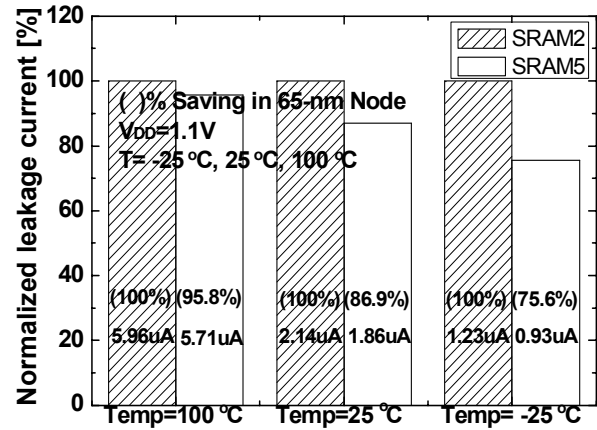


(b)

Figure 12. Oxide-tunneling leakage of the MN3, MN4 and the cell of the SRAM5 with the 32-nm PTM at (a) 100°C and (b) 25°C

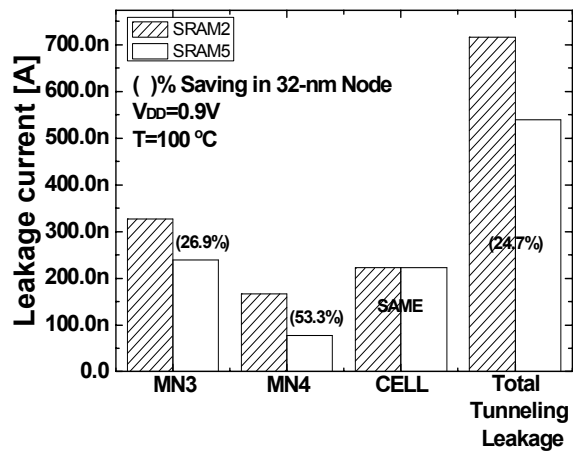


(b)

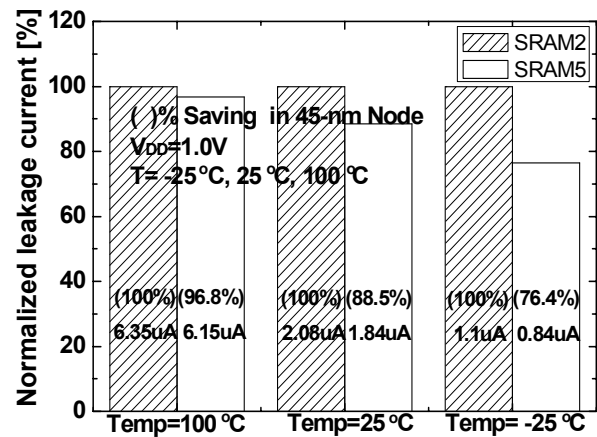


(a)

Figure 11. Oxide-tunneling leakage of the MN3, MN4 and the cell of the SRAM5 with the 45-nm PTM at (a) 100°C and (b) 25°C



(a)



(b)

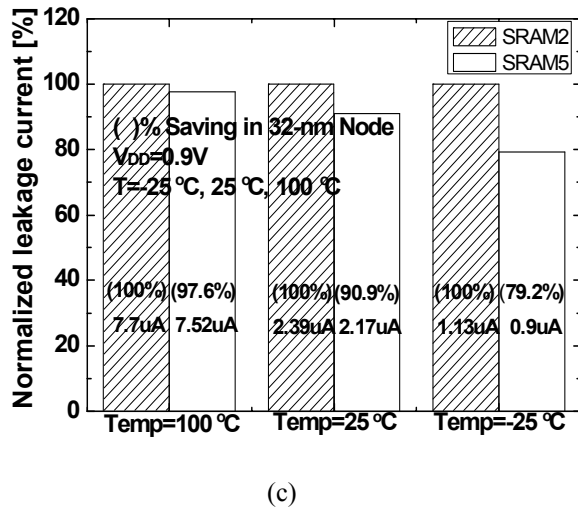


Figure 13. Comparison of the normalized leakage currents of the SRAM2 and the SRAM5 at -25°C, 25°C, and 100°C with (a) the 65-nm, (b) the 45-nm, and (c) the 32-nm PTMs

V. CONCLUSIONS

In this paper, we compare the four SRAM circuits. They are the conventional SRAM1, the SRAM2 with power gating on the V<sub>SS</sub> line, the SRAM3 with power gating on the V<sub>DD</sub> line, and the SRAM4 both on the V<sub>DD</sub> and V<sub>SS</sub> lines, respectively. Among the four SRAMs, the SRAM2 shows the smallest amount of leakage, because its subthreshold leakage is most suppressed by its BODY and DIBL effects. In addition, the area overheads of the SRAM2, SRAM3, and SRAM4 are also compared and discussed.

To reduce the oxide-tunneling leakage of the SRAM2 more, the SRAM5 with its precharge voltage lowering is studied in this paper. Compared with the SRAM2 without lowering of the precharge voltage, amounts of leakage of the SRAM5 are suppressed by 24.4%, 13.1%, and 4.2%, respectively, at -25°C, 25°C and 100°C, for the 65-nm node.

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