

High performance Flying Capacitor based Multilevel Inverter fed Induction Motor

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Abstract— The paper presents a high performance flying capacitor fed induction motor drive. To improve the performance of Flying Capacitor Multilevel Inverter (FCMLI) implement the switching pattern selection scheme. This scheme reduces capacitor voltage fluctuation without using voltage feedback. This method is developed for sinusoidal voltage generation using the sinusoidal pulse width modulation technique and was compared favorably with the result when voltage feedback was used.

Index Terms— AC Drive, Flying capacitor, Multi level inverter. Total Harmonic Distortion (THD).

I. INTRODUCTION

The multilevel voltage source inverter is recently applied in many industrial applications such as AC power supplies, static VAR compensators, drive systems etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [1-3]. The output voltage waveform of a multilevel inverter is composed of number of levels of voltages, typically obtained from capacitor voltage sources. As the number of levels reach infinity, the output THD approaches nearly zero [4]. The number of achievable voltage levels, however is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

Maynard and Foch introduced a flying-capacitor-based inverter in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place.

Three types of multilevel Inverter

1. Diode-Clamped Multilevel Inverter.
2. Flying-Capacitor Multilevel Inverter.
3. Cascaded-Multi Level Inverters.

II. FLYING CAPACITOR MULTILEVEL INVERTER

The FCMLI requires a large number of capacitors to clamp the device (switch) voltage to one capacitor voltage level. Provided all the capacitors are of equal value, an n -level inverter will require a total of $(n-1) \times (n-2)/2$ clamping capacitors per phase leg in addition to $(n-1)$ main dc bus capacitors. The size of the voltage increment between two consecutive legs of the clamping capacitors defines the size of voltage steps in the output waveform. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor, then for an n level inverter, if the voltage of the main dc-link capacitor is V_{dc} , the voltage of the innermost capacitor clamping the innermost two devices is $V_{dc}/(n-1)$.

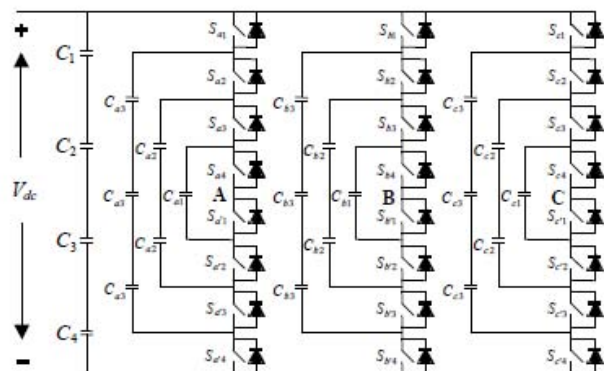


Figure 1. Three phase five level capacitor inverter.

The voltage of the next innermost capacitor will be $V_{dc}/(n-1) + V_{dc}/(n-1) = 2V_{dc}/(n-1)$ and so on. Each next clamping capacitor will have the voltage increment of $V_{dc}/(n-1)$ from its immediate inner one. The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assures that the voltage stress across each main device is same and is equal to $V_{dc}/(n-1)$, for an n -level inverter. Figure 1 shows one phase leg of a 5-level inverter. For a 3-phase inverter, two more legs of same

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construction are coupled to the same dc-link battery V_{dc} . In this figure each switch S_{a1} to S_{a4} and $S_{a'1}$ to $S_{a'4}$ consists of a power semiconductor device (e.g. GTO, IGBT) and an anti-parallel diode. Voltages V_{C1} , V_{C3} , V_{C2} and V_{C4} are $V_{dc}/4$, $V_{dc}/2$, $3V_{dc}/4$ and V_{dc} respectively, as $n = 5$.

The switch combinations given in Table 1 is used to synthesize the output voltage of phase-a, V_{an} , with respect to the neutral point n . The main dc capacitor combination, C_1 is the energy storage element, while capacitors C_2 , C_3 and C_4 are the flying capacitors that provide the multilevel voltage ability to the converter. The pairs of the switches (S_1, S_{11}), (S_2, S_{21}), (S_3, S_{31}) and (S_4, S_{41}) are closed in complementary manner. Thus if S_1 is ON, S_{11} is OFF and vice-versa.

TABLE.1 SWITCHING SCHEME FOR ONE PHASE LEG OF A 5-LEVEL FCMLI

S1	S2	S3	S4	C2	C3	C4	V_{an}
ON	ON	ON	ON	NC	NC	NC	$V_{dc}/2$
ON	ON	ON	OFF	NC	NC	+	$V_{dc}/4$
ON	ON	OFF	ON	NC	+	-	
ON	OFF	ON	ON	+	-	NC	
OFF	ON	ON	ON	-	NC	NC	
OFF	OFF	ON	ON	NC	-	NC	0
OFF	ON	OFF	ON	-	+	-	
OFF	ON	ON	OFF	-	NC	+	
ON	OFF	OFF	ON	+	NC	-	
ON	OFF	ON	OFF	+	-	+	
ON	ON	OFF	OFF	NC	+	NC	
ON	OFF	OFF	OFF	+	NC	NC	$-V_{dc}/4$
OFF	ON	OFF	OFF	-	+	NC	
OFF	OFF	ON	OFF	NC	-	+	
OFF	OFF	OFF	ON	NC	NC	-	
OFF	OFF	OFF	OFF	NC	NC	NC	$-V_{dc}/2$

In Table 1, NC indicates that there is no change in the state of corresponding capacitor, i.e. the capacitor neither charges nor discharges in this mode. The states + and - respectively denote the charging and discharging of the corresponding capacitors. The switching states given are for the positive half cycle of the outgoing current waveform. The capacitor states (+ and -) will reverse for the negative half cycle of the current. From table 1 that the structure offers multiple switching combinations for V_{an} equal to $V_{dc}/4$, 0 and $-V_{dc}/4$. Calculated for any initial state of clamping voltages the inverter output voltage is given by

$$V_{an} = S_1 (V_{C1} - V_{C2}) + S_2 (V_{C2} - V_{C3}) + S_3 (V_{C3} - V_{C4}) + S_4 (V_{C4} - V_{C1}) / 2$$

III. MODULATION SCHEME

The various switching strategies that have been proposed for synthesizing output voltage with minimum distortion, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method, a number of triangular waveforms are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by the intersection of the carrier waves with the modulating signal. For a 5-level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter as shown in Figure 2.a The modulating signal of each phase is displaced from each other by 120° . All of the carriers have the same frequency f_c and the same amplitude A_c , while the modulating signal has a frequency of f_m and amplitude of A_m . f_c should be in the multiples of three-times to that of f_m . This is required such that all the modulating signal of all the three phases see the same carriers, as they are 120° apart.

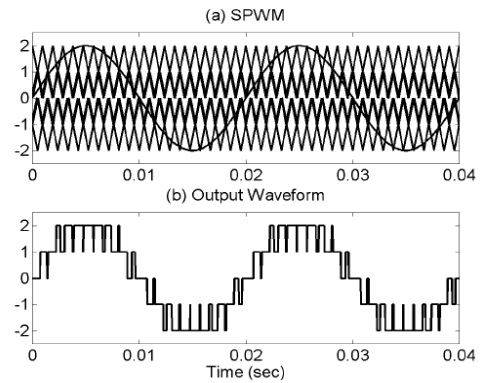


Figure 2. Waveform of SPWM and output voltage

The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from + 2 to - 2. The amplitudes of the 4 carrier waves vary from 0 to 1, 1 to 2, in the positive half cycle of the modulating signal, and from 0 to - 1, and - 1 to - 2 in the negative half cycle. In the positive half cycle the output will have the value + 1 if the amplitude of the modulating signal is greater than that of the carrier wave (0 to 1) and 0 otherwise. Similarly for the negative half cycle if the modulating signal is lower than the carrier wave (0 to -1), the output of the comparator is - 1 and 0 otherwise. If the modulating signal is greater than both the carrier waves in the positive half, the output is + 2. In this way 5 output levels (+ 2, + 1, 0, - 1, - 2) are obtained. The outputs of each comparator for each phase are combined to produce the corresponding decision signals for the switches to synthesize the output voltage of that phase. The SPWM output reference signal is shown in Figure 2.b. This signal resembles the output voltage waveform of the inverter

and decides the voltage level, which is to be generated at a particular instant.

IV. SIMULATION RESULTS

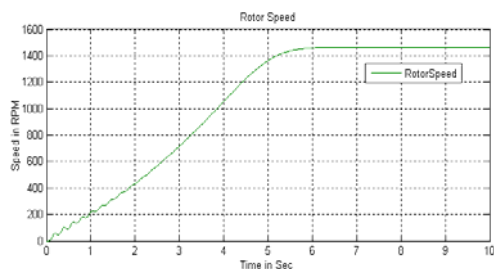


Figure 3. Speed of the motor.

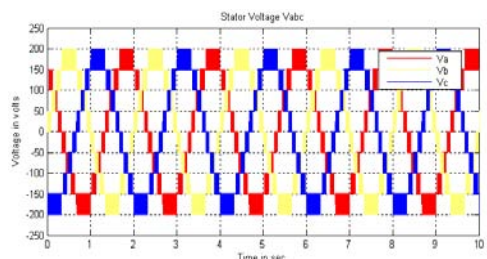


Figure 4. Stator Voltage (V_{abc}) Vs Time.

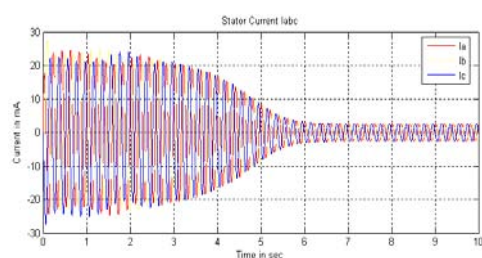


Figure 5. Stator Current (I_{abc}) Vs Time.

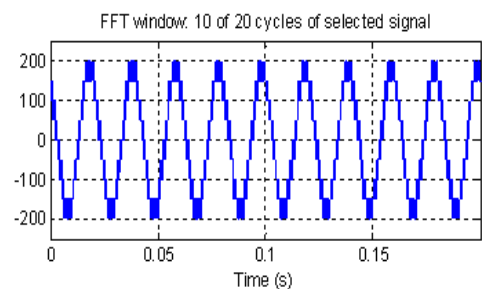


Figure 6. Output voltage for FFT window.

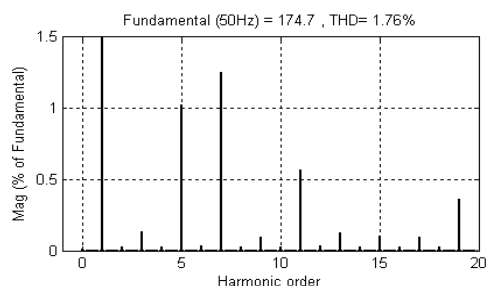


Figure 7. FFT harmonics spectrum.

V. RESULT ANALYSIS

Speed of the induction motor is shown in figure 2. When the settling speed is quick response and gets 1440 rpm. Stator voltage of the flying capacitor as shown in figure 4. The voltage should be 5 levels and the amplitude 200 voltage. The inverter voltage gets nearly sinusoidal. Hence the harmonics and motor oscillation will be reduced.

The stator current waveform of flying capacitor is illustrated as Figure 5. It takes high starting current and minimum in running condition. Lower order harmonics are significantly reduced.

The output voltage of FFT window illustrated the figure 6. The voltage amplitude is 200 volts and minimum harmonics. Finally the figure 7 shows FFT harmonic spectrum of flying capacitor is 1.76%

CONCLUSIONS

In the proposed five levels flying capacitor multilevel inverter is used to get sinusoidal waveform and also increase the efficiency of the inverter. The five level inverter has been illustrated in simulation results by using MATLAB. The inverter is low means the design of the inverter switching pattern is easiest. Multilevel inverter is to obtain a high resolution. The technique is used to improve the level of inverter and extends the design flexibility and reduced the harmonics.

REFERENCES

- [1] J. L. Thomas, S. Poullain, A. Donzel, and G. Bornard, "Advanced torque control of induction motors fed by a floating capacitor multilevel VSI actuator", IEE Seminar, 'Advances in Induction Motor Control', 23 May, 2000, pp. 5/1 - 5/5.
- [2] T. A. Meynard, M. Fadel and N. Aouda, "Modeling of multilevel converters", IEEE Transactions on Industrial Electronics, Vol. 44, No. 3, June, 1997, pp. 356 - 364.
- [3] T. A. Meynard, and H. Foch, "Multi-level choppers for high voltage applications", EPE Journal, Vol. 2, No. 1, March 1992, pp. 45 - 50.
- [4] G. Gateau, P. Maussion, and T. A. Meynard, "Fuzzy phase control of series multicell converters", Proceedings of the 6th IEEE International Conference on Fuzzy Systems, 1 - 5 July, 1997, Vol. 3, pp. 1627 - 1633.
- [5] Fukuda, S. and Suzuki, K, "Using harmonic determination factor for harmonic evaluation of carrier-based PWM methods", Conference Record of IAS '97, IEEE Industry Applications Society 32nd Annual Meeting, 5 - 9 October, 1997, pp. 1541 - 1541.
- [6] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: active control and observation of flying capacitor voltages", IEEE Transactions on Industrial Electronics, Vol. 49, No. 5, October 2002, pp. 998 - 1008.
- [7] F. G. Turnbull, "Selected harmonic reduction in static d-c - a-c inverters", IEEE Transactions on Communications and Electronics, Vol. 83, July 1964, pp. 374 - 378.
- [8] Enjeti, P. and Lindsay, J.F., "Solving nonlinear equations of harmonic elimination PWM in power control", IEE Electronic Letters, Vol. 23, No. 12, June 1987, pp. 656 - 657.