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Implementaion of Current Commutation Strategies of Matrix Converters in FPGA and Simulations Using Max+PlusII

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Abstract—**There has been recently considerable interest in the use of matrix converters as a good alternative to the rectifier/PWM-inverter combination, particularly in electric drive applications. However, the reliable current commutation for switches in a matrix converter is a difficult task and may adversely affect the quality of output waveforms. In this paper, different current commutation strategies are studied and discussed in terms of features. Then, the implementation of these strategies on FPGA is addressed to get outputs of higher quality. Also the implementation is simulated and tested by using MAX+PLUSII.**

Index Terms—**Matrix Converter, Current Commutation strategies, Simulation, FPGA, VHDL.**

I. INTRODUCTION

The Matrix Converter (MC) concept was first published in 1976 [1]. The circuit was actually a new form of cycloconverters where the devices were fully controllable. Hence, the MC is sometimes called a forced commutated cycloconverter. A lot of research interest followed the publication of Venturinis' first paper of 1980 [2] which put the MC control and modulation algorithms on a mathematical foundation. The MC offers an all-silicon solution for AC-AC power conversion without any energy storage element. The circuit consists of an array of bidirectional switches arranged so that any of the output lines of the converter can be connected to any of the input lines. Fig. 1 shows a typical three-phase to three-phase matrix converter with nine bidirectional switches. This configuration is mostly called direct converter while an indirect one is similar to a rectifier/PWM-inverter without any energy storage element at DC link.

The proper output waveforms are then generated by using a suitable PWM pattern. An input filter is used to remove harmonic components. The MC has many advantages over traditional AC-AC converter topologies. It is inherently bidirectional and can regenerate energy back to the utility. It draws sinusoidal input currents, and depending on the modulation technique, can be arranged to produce a unity displacement factor at the utility side regardless of the load type. The converter size has the potential to be considerably smaller than conventional topologies since there is no large capacitor or inductor to store energy [3]. The main disadvantages of the MC are: the lack of any discrete device in the market to function as a bidirectional switch resulting in a large number of discrete power switches to be used for implementation of such switches; a low maximum voltage transfer ratio; and the difficulty in current commutation of any two switches without resulting overcurrents and/or overvoltages. These negative perspectives have stopped the MC to be widely used in practice. There are a number of current commutation strategies presented in the recent publications which yield the least stress on the switches.

These strategies are reviewed here and their features are discussed. On the other hand, because of the fast computational capability and low cost of field programming gate arrays (FPGAs), they have recently attracted a lot of interest to be used in motor drive applications. The implementation of current commutation strategies on the FPGA are then addressed and simulated.

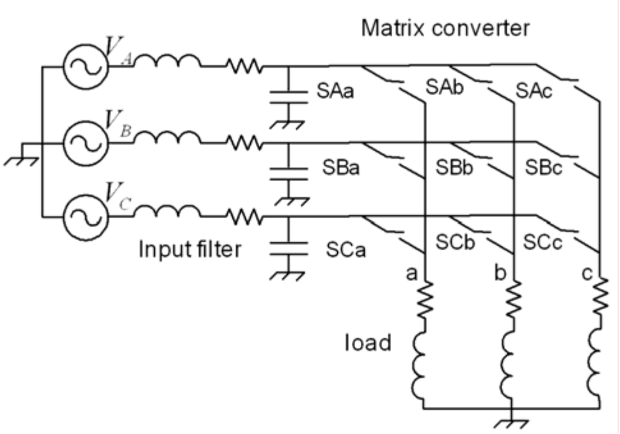
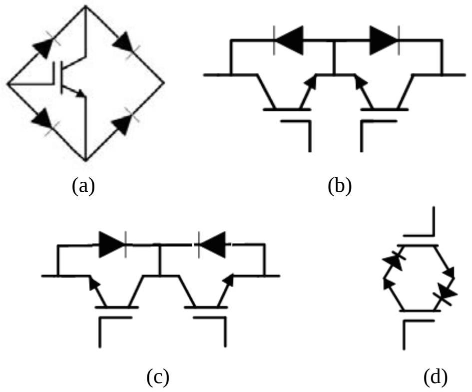


Figure 1. The basic MC power circuit

II. BIDIRECTIONAL SWITCHES

The MC requires bidirectional switches capable of blocking voltage and conducting current in both directions. Unfortunately, there is no discrete semiconductor device currently available in mass-production that fulfils the above requirements. Therefore, the accessible discrete devices need to be used to construct suitable bidirectional switch cells. There are four arrangement commonly used to create a bidirectional switch as shown in Fig. 2. It is assumed here that the switching device is an IGBT (Insulated Gate Bipolar Transistor), but other devices such as MOSFETs (Metal

Oxide Semiconductor Filed Effect Transistors), MCTs (MOS Controlled Thyristors) and IGCTs (Integrated Gate Commutated Thyristors) can be used in the same way where they are more applicable. Fig. 2(a) shows a diode full bridge with one switching device providing the current path for both directions. This arrangement has the advantage of requiring only one IGBT and its associated gate driver circuit. The main disadvantage of this arrangement is that three devices are conducting at any given time, resulting in relatively high conduction losses. Common emitter arrangement shown in Fig. 2(b) consists of two diodes and two IGBTs connected in anti-parallel. The diodes provide the reverse blocking capability and the possibility to independently control the direction of the current. Each bidirectional switch requires an isolated power supply for the gate driver in the direct configuration, but both devices can be driven with respect to the same voltage, namely the common emitter point. Common collector arrangement shown in Fig. 2(c) is similar to the previous one, but the IGBTs are arranged in a common collector configuration. The conduction losses are the same as the common emitter arrangement. The advantage of this method is that only six isolated power supplies are needed to supply the gate drivers of a complete three phase MC. However, this arrangement is often not feasible in a large practical system since inductance between commutation cells causes problem. In many implementations of MCs, the common emitter arrangement is mostly used, because the smaller size of a complete high power converter and lower parasitic inductance are of its advantages. A new device called Reverse Blocking IGBT (RBIGBT) offers a simple anti-parallel structure for bidirectional switches as shown in Fig. 2(d) with excellent conducting losses and all positive features of the other arrangements described above. But the switching losses of RBIGBTs are rather high. So it will decrease the switching frequency, resulting in a larger filter design [4]. There are three possible ways to package bidirectional switches used in the MC.


(a) (b)

(c) (d)

Figure 2. Different arrangements of the bidirectional switch:
(a) one diode full bridge and one switch
(b) common emitter switches and anti-parallel diodes
(c) common collector switches and anti-parallel diodes
(d) anti-parallel reverse blocking switches

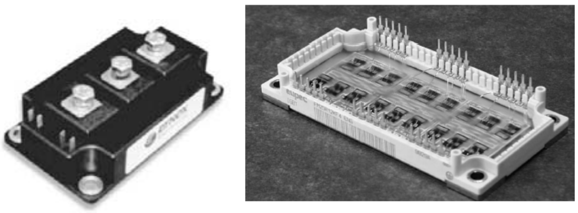

(a) (b)

Figure 3. Bidirectional switches packaging (a) 400A single switch module DIM200MBS12 made by Dynex (b) 7.5kW MC module EconoPack 3 made by EUPEC

For higher power converters, each bidirectional switch can be packaged separately in a module similar to that used for an individual inverter leg. An example is a 400A bidirectional switch module made by Dynex shown in Fig. 3(a). It is also possible to build a complete output leg of the MC by rearranging the interconnection of devices in a standard six–pack IGBT module, giving the converter a greater power density levels and lower stray inductances. For low power MCs, it is possible to build a complete converter in a single package. This packaging is shown in Fig. 3(b), a 7.5kW module made by EUPEC.

III. CURRENT COMMUTATION STRATEGIES

A. *Commutation based on current direction*

One reliable method of current commutation, which obeys the aforementioned rules, uses a four-step commutation strategy in which the direction of current flow through the commutation cells can be controlled. In order to explain this strategy, a two-phase to single-phase MC is considered as shown in Fig. 4. It should be noted that based on the rules the following conditions should be avoided:

- S_{1a} and S_{2b} are both on when $V_A>V_B$
- S_{2a} and S_{1b} are both on when $V_A<V_B$

The four-step commutation method based on the load current direction includes the following stages:

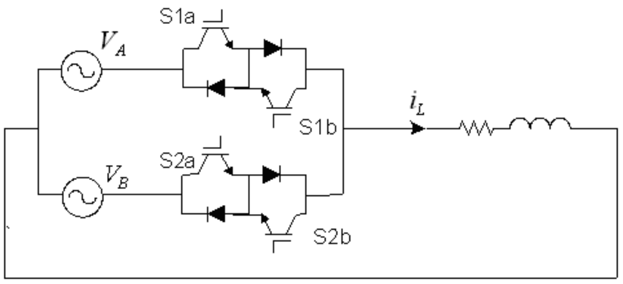
a) Suppose that initially S1 is on, S2 is off and $i_L>0$. That means S1a and S1b are on, and S2a and S2b are off. It is necessary to turn S1 off and S2 on. Therefore, S1b is turned off. This brings no overcurrent problem, since there is no current flow through S1b and the load current is not interrupted.

b) S2a is switched on. It can conduct the current if $V_A < V_B$.

c) S1a is switched off. If S2a was not actually conducting, there would be an overvoltage due to the load current flow interruption, which eventually leads to the current conduction of S2a. Note that this completes the commutation process. Now, S1 is off and S2 is on.

d) S2b is switched on. This enables S2 to conduct the load current in both directions.

The above stages are shown by a timing diagram in Fig. 5. The delay between each switching event is determined by the device characteristics. Fig. 6 shows a state diagram of the four-step commutation strategy for one output phase. The commutation sequence is dependent on the current direction, which has to be monitored by the commutation control logic [5].



(a) (b)

Figure 4. Two-phase to single-phase MC

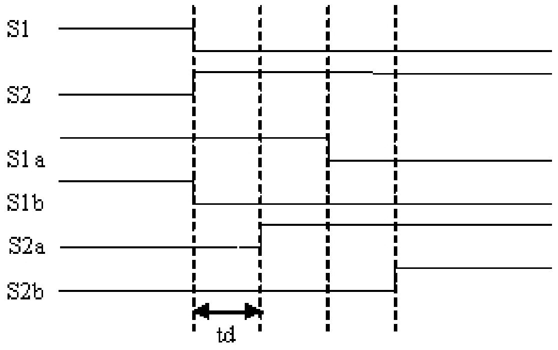


Figure 5. Timing diagram for four-step current commutation strategy

An alternative method is a two-step current commutation strategy. In this method, only the device carrying the current and the device becoming the next current carrying one are gated at any given time. So, the first and last stages in the above procedure are leaved out. All the current commutation techniques in this category rely on the knowledge of output line current direction. This can be difficult to reliably determine in a switching power converter, especially at low current levels in high power drives. To avoid this problem, a technique using the voltage across the bidirectional switch has been employed to determine the current direction.

Assume that V_1 denotes the forward voltage across the discrete switch S_{1a} and V_2 would be the forward voltage across the discrete switch S_{1b}. V_1 and V_2 will be respectively positive and negative when S_1 is conducting a positive load current as shown in Fig. 4. If the load current is negative, V_1 and V_2 will be respectively negative and positive. So, the measured voltages across each half the bidirectional switch can reveal the load current direction. All methods described above can be implemented in a relatively inexpensive digital gate array such as a FPGA.

B. Commutation based on voltage magnitude

An alternative approach of the current commutation relies on knowledge of the relative magnitude of the input voltages instead of considering the direction of the output current. The switches are then opened to block the reveres voltages. From this information a two-step or four-step voltage-magnitude-based current commutation strategy can be developed in a similar way to the two-step or four-step current-direction-based commutation techniques. As an example, assume that the load current flows in the direction shown in Fig. 4, and S_1 is closed. When a commutation to S_2 is required, the relative values of V_A and V_B are compared to each other and the switching sequence for a four-step commutation method is determined based on the following rules:

If $V_A > V_B$: first, S_{2a} is switched on, next, S_{1a} is switched off, next, S_{2b} is switched on, and finally, S_{1b} is switched off.

If $V_A \le V_B$: first, S_{2b} is switched on, next, S_{1b} is switched off, next, S_{2a} is switched on, and next, S_{1a} is switched off

The current commutation methods based on input voltage magnitude have the advantage that the measured voltages are independent of the load current level and the measuring is practical for a complete MC package or a complete leg of the MC package when there is no access to internal connection points.

IV. IMPLEMENTATION IN FPGA

A FPGA is a semiconductor device consisting of programmable logic components called *logic blocks*, and programmable interconnections. *Logic blocks* are to have the function of basic logic gates. *Logic blocks* and interconnections are to be programmed by the customer or designer after the FPGA is manufactured (hence it is field-programmable). FPGAs were introduced as an alternative to custom ICs for implementing the glue logic, because of its improved density relative to the discrete components, the reduced system complexity, the low manufacturing cost and the improved performance. Using a computer aided design (CAD) tool, circuits could be arranged in a short time frame, because no physical layout process and no masking are required. Fig. 7 shows a FPGA in the loop in order to implement the current commutation methods for MCs. Generally, current commutation methods can be implemented in a FPGA to increase the speed of switching sequence and commutation process for high frequency applications. As shown, the output of a current sensor is applied as the input to the FPGA to determine the load current direction, and the outputs of the FPGA are applied to the gate derivers [6].

As seen from Fig. 6, there are three stable states for the MC, and the commutation sequence depends on the current direction. Therefore, there are totally six bidirectional paths, or twelve unidirectional paths for all possible switching states. The VHDL code is used to implement the current-direction-based commutation method on FPGA. To describe the code for a four-step commutation, the flowchart of VHDL program is shown in Fig. 8.

For example, suppose a positive load current flowing into the load and an incoming commutation switching to state 2 (001100) as a new state. If the current stable state is state 1 (110000), this algorithm will compare the current state to the new state, and according to the actual current direction, the correct transient path will be determined. So it will be a transient path to 10-00-00, to 10-00-10 and finally to 00-00-01.

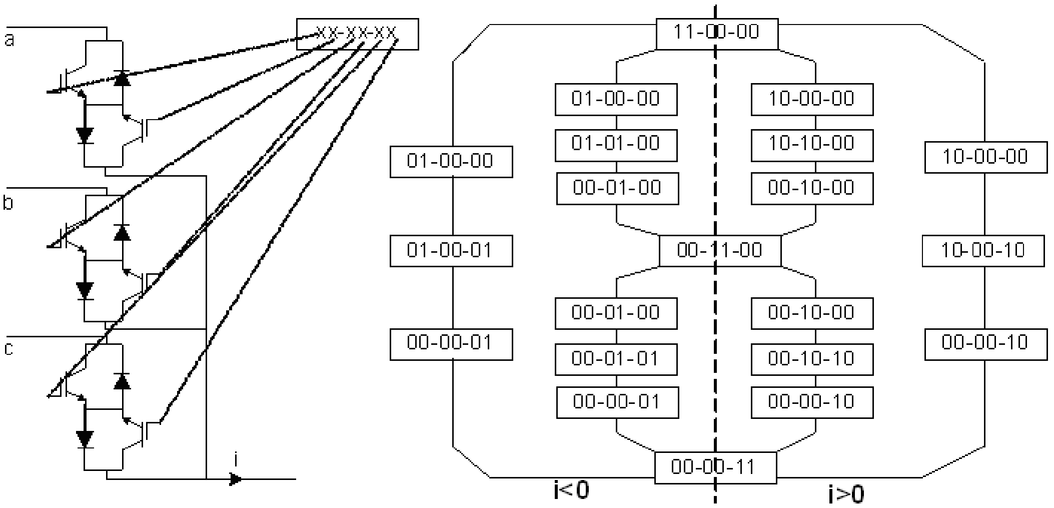


Figure 6. Logic state-diagram of a four-step current-direction-based commutation method for one output phase

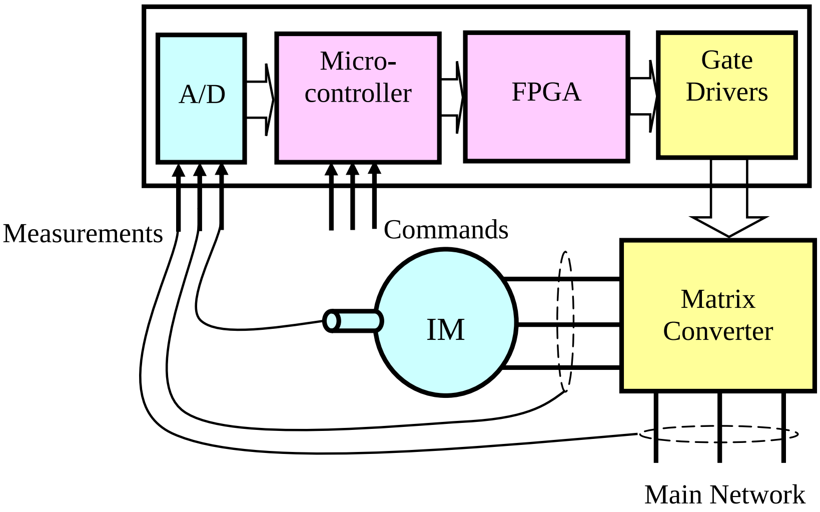


Figure 7. FPGA in the loop as current commutation commander for a matrix converter

V. SIMULATION BY MAX+PLUSII

The software of MAX+PLUSII is a fully integrated programmable logic design environment used widely to estimate the performance of programmed logic arrays. This easy-to-use tool supports the Altera® FLEX® and MAX® programmable device families, and works with both Microsoft Windows and UNIX. MAX+PLUSII offers considerable flexibility and performance, and allows effective integration to industry-standard design, synthesis and verification. The four–step current-direction-based commutation method is simulated here by MAX+PLUSII. In the VHDL code, the current state is denoted by *stateout* and the next one by *newstate*. $i=0$ implies that the current is negative (i.e. $i<0$ as flowing from the load to main network) and $i=1$ means that the current is positive ($i>0$ as flowing into the load).

Fig. 9 shows the results of the VHDL simulation for switching from state 11-00-00 to state 00-11-00. The new commutation switching state is state 2 (00-11-00). This state will be compared with the current state (state1), and the transient path will be chosen according to the flowchart in Fig. 8. For a negative current, the four-step commutation follows a transient path from state 11-00-00 to state 010000, to state 010100, to state 000100, and finally to state 001100. At the end of the commutation process, the current state is replaced by the state2. Fig. 10 shows the results of VHDL simulation for switching from state 00-00-11 to state 11-00-00.

In Fig. 9 and 10, the sign of current direction (*i*), input clock pulse (*clk*), command of switching between current state and next state (*newstate*) and switching stages as the output of FPGA (*stateout*) are shown. When a command starts at one down edge of the clock pulse, four transient state changes are occurred in successive up edges of the clock pulse. The switching frequency is about 1 MHz as determined by the time period of the input clock pulse. Therefore, the total transition takes less than 3.5 μs. The whole switching time changes with a change in the time period of the input clock pulse. So a very fast signaling to gates is achievable.

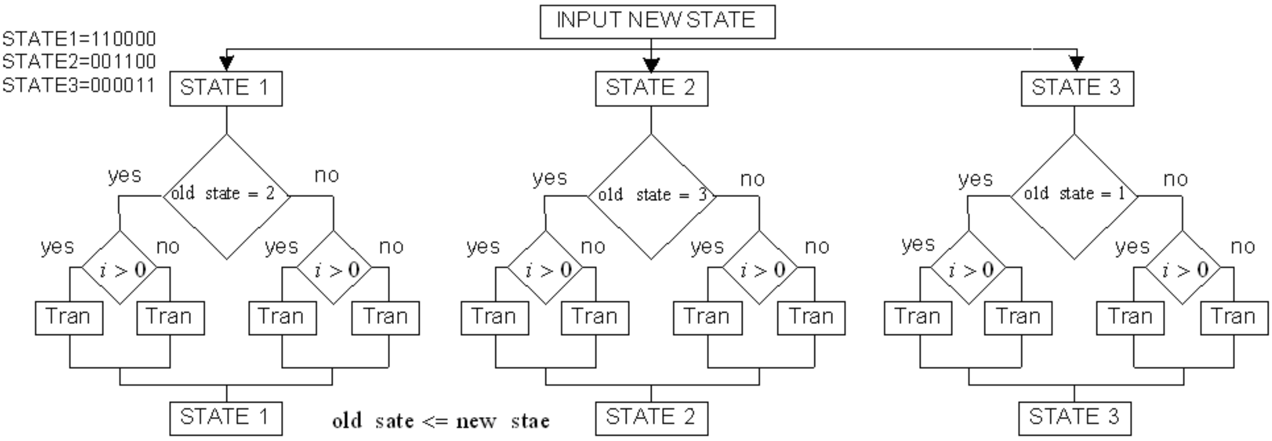
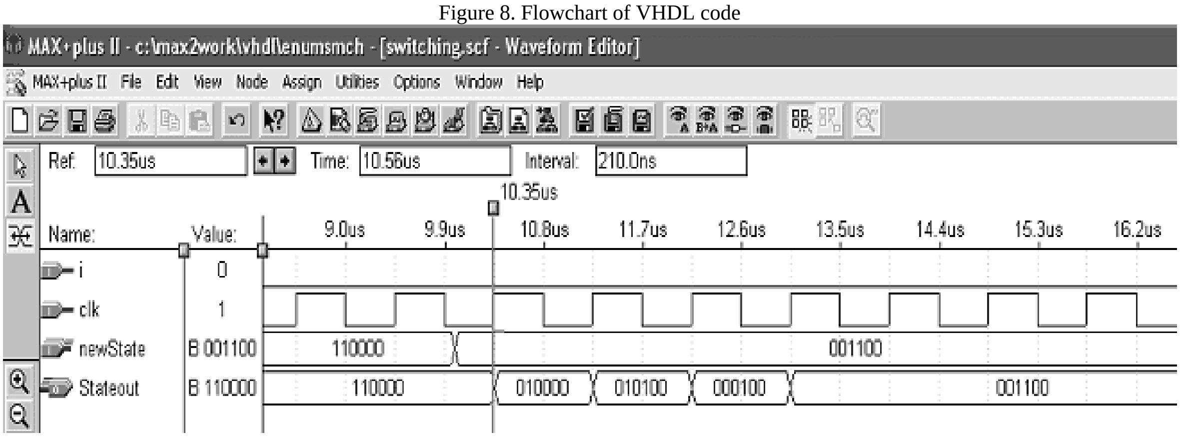


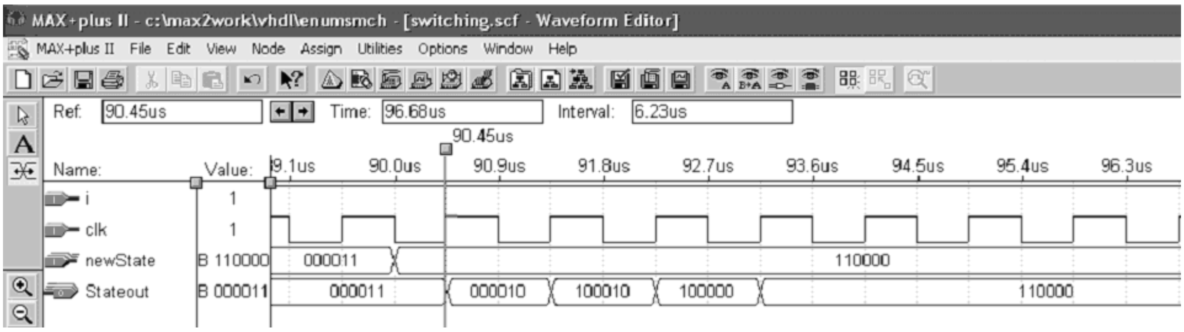
Figure 8. Flowchart of VHDL code



Ref: 10.35us Time: 10.56us Interval: 210.0ns

Name:	Value:					
i	0					
clk	1					
newState	B 001100	110000	001100			
Stateout	B 110000	110000	010000	010100	000100	001100

Figure 9. Results of VHDL simulation for switching from state 110000 to state 001100



Ref: 90.45us Time: 96.68us Interval: 6.23us

Name:	Value:					
i	1					
clk	1					
newState	B 110000	000011	110000			
Stateout	B 000011	000011	000010	100010	100000	110000

Figure 10. Results of VHDL simulation for switching from state 000011 to state 110000

VI. CONCLUSIONS

The paper reviews different current commutation strategies used in matrix converters to avoid overvoltage and overcurrent stresses on bidirectional switches. Next, the implementation of these strategies in FPGA is addressed to achieve high speed signaling to gate for high frequency applications such as high performance electric drives.

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