

# Comparative Analysis of Different ADC parameters used in software radio for Mobile receiver

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**Abstract:** In recent years, there has been an explosive demand for wireless and portable applications, which resulted in more flexible communication systems that can handle various standards in different environments. In an ideal software radio, the data conversion occurs immediately after the signal received from the receiving antenna. This paper presents multi-standard reconfigurable modulators, which are able to support the predictable standards of fourth generation of mobile communication systems (4G). While designing software radio the selection of analog to digital converter is one of the most challenging step. Present paper also discusses the role of different ADC parameters in the optimum design of software radio.

**Keyword:** Analog to Digital Converters (ADC), Software Defined radio (SDR), SNR, Intermediate Frequency (IF), Radio frequency (RF).

## I. INTRODUCTION

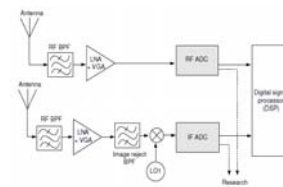
A software defined radio adopts a fully reconfigurable front end and is believed to be the right answer to realize 3G/4G mobile systems [4]. The rapid development of digital wireless system, led to a need for high resolution and high speed band pass analog to digital converters. Continuous time band pass Sigma delta modulator are very suitable for such high frequency applications [1]. Performance of the sigma delta ADC with various parameters will be evaluated in terms of SNR. The signal to noise ratio (SNR) is defined as the ratio of the signal power to the signal integrated noise power over the signal bandwidth. It is related to its resolution (no. of bits N),

$$\text{SNR}(\text{db}) = 6.02 * N + 1.76 \text{db} \quad (1)$$

Another performance measure of an ADC is the dynamic range (DR), which is defined as the ratio between maximum input signal power with acceptable distortion in the minimum detectable input signal power level. In section III, Classification of ADC architecture based on speed & resolution is given. In section IV various parameters of ADCs are discussed. It is concluded in section V, References are given in section VI.

## II. ADC for Software Radio Communication Receivers

The viability of the receiver and transmitter structures depends on suitable interfaces between analog and digital domain in order to push the boundary between analog and digital domain towards higher IFs or even beyond. Both the ADC & DACs requires a sufficiently high sampling rate further more high resolution in terms of the quantizer's word length which is important for achieving a large dynamic range [2].



Figure(a) ADC for software radio communication receivers

Additionally low sampling jitter, good linearity and low power consumption and cost are further desirable properties. Figure(a) shows the block diagram of a receiver.

The optimization of such a receiver depends strongly on the obtained Dynamic Range and SNR in the ADC [2].

## III. CLASSIFICATION OF ADC ARCHITECTURE

The different categories of the ADC architectures based on their speed, resolution and power. The flash, folding, sub ranging and pipeline ADC architectures are in the very high speed and medium to low resolution category, while the successive approximation and sigma delta ADC architecture are in the high/medium speed and high resolution category. The sigma delta ADC is the only architecture in the over sampled category, while all the other architectures belong to the Nyquist rate category [3].

### A. Nyquist rate analog & Digital converters

The process of sampling of a continuous time analog signal  $x(t)$  at a frequency  $f_s$  (time period  $=T_s = 1/f_s$ ) in ADC is equivalent to multiplexing the signal by impulse trains that repeat every  $T_s$  seconds. Mathematically, the sampled discrete time signal is given in time domain by

$$x^*(t) = \sum x(t) \delta(t - nT_s) \quad (2)$$

Where  $n$  is integer and  $\delta$  is the ideal impulse function. The quantization noise power of Nyquist rate, ADC extends in frequency from DC to  $F_s/2$ .

### B. Over sampled or Sigma Delta ADCs:

The ADC architecture that have a sampling frequency much greater than that the Nyquist sampling criteria belong to the category of over sampled ADC. The basic components of a  $\Sigma\Delta$  ADC includes a loop filter in the forward loop followed by a comparators, with a feedback digital to analog converters (DAC) computing the negative feedback loop as shown in figure (b).

While considering a small signal model and assuming a unity transfer function for the DAC and comparator, the

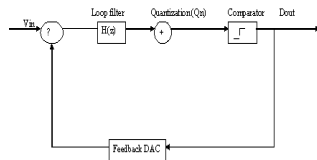


Fig .(b). Block Diagram of a  $\Sigma\Delta$  ADC output ( $D_{out}$ ) is given by

$$D_{out} = STF * V_{in} + NTF * Q_n \tag{3}$$

Where  $Q_n$  is quantization noise, STF & NTF are the signal and noise transfer functions. The STF and NTF of the ADCs are given by

$$STF = D_{out}/V_{in} = H(z)/(1+H(z)) \tag{4}$$

$$NTF = D_{out}/Q_n = 1/(1+H(z)) \tag{5}$$

The digital output ( $D_{out}$ ) then passes through decimation and digital filter blocks, where down sampling is performed to get the final output.

**C. Band pass sigma-delta analog to digital converters**

A band pass  $\Sigma\Delta$  ADC is obtained by replacing  $H(z)$  with a band pass filter. The analog signals that have to be digitized in software radio receivers are located at center frequency  $F_0$  and the signal bandwidth is  $SB$ . The quantization noise is attenuated only in the required signal bandwidth instead of the whole Nyquist bandwidth, which implies lesser power consumption to obtain similar dynamic range as compared to a Nyquist converter. Bandpass sigma delta ADC architecture is the best choice for digitization in software radio receivers [2].

**IV. VARIOUS PARAMETERS OF ADC:**

ADC must perform two fundamental steps: Sampling and quantization. Sampling changes a signal that exists continuously in time to a signal that is non zero only at discrete instances of time. An ideal software radio would use data converters at RF, which would result in conflicting needs: a very high sampling rate, a bandwidth up to several GHz and a high effective dynamic range while avoiding intolerable power consumption.

**Practical timing issues**

The performance of a data converter is dependent upon the accuracy and stability of clock supplied to the circuits. When data converter employ a high sampling rate, clocking issue become magnified and significant distortion can result. Two of the most significant timing issues are aperture jitter and clock jitter[6] .

Clock Jitter is defined as the instability of the sampling clock which is caused by phase noise of the oscillator. Several author have tried to model the band pass  $\Sigma\Delta$ ADCs and clock jitter .*Hairong chang & Hua Tang* described a simple and effective Technique is reduce clock jitter effect in CT  $\Delta\Sigma$  Modulator [14].

Aperture Jitter is the limiting effect in ADCs with a digitization bandwidth between 1MHz and 1GHz. In [3] Walden identified the aperture jitter as the dominating error

effect that limits the resolution of wideband ADC (with digitization bandwidths between 1MHz and 1GHz).Walden used a worst case approach. *Kobavashi* presented an exact formula which allows to calculate the SNR in the presence of an aperture jitter [5].V.Chris Flakes presents a quantitative analysis of some basic parameter of an ADC. The ADC performance improves only by decreasing aperture jitter [12].

**TABLE I**  
Simulated performance for different standards

Paper		BW (MHz)	OSR	SNR (dB)	Jitter tolerance	Estimated Power
[12]	WLAN	20	16	59	10 ps	8 mw
	DVB-H	3.8	24	68.5	12 ps	3.5 mw
	UMTS	2	32	77	9 ps	3 mw
	GSM	0.2	128	84.5	5 ps	2 mw

The simulated performance using Matlab is given and summarized in Table I. It shows the better power efficiency.

**Quantization:**

Quantization is the process of mapping a continuous valued signal into a discrete set of levels. In data converters. The quantization process is characterized by a few simple parameters: the number of a quantization levels, the range of quantizable input voltages, and the width of quantization level plays an important role in many systems where analog-to-digital conversion takes place. If the quantization error is correlated with the input signal, then the spectrum of the quantization error will contain spurious peaks[16].The number of levels in the discrete set is determined by the number of bits  $B$  used and is given by

$$\text{Number of quantization levels} = 2^B. \tag{5}$$

Quantization error,  $e(x)$ , is defined as the difference between the quantized (discrete valued) signal,  $x_Q$  and original (continuous) signal  $x$ . Its instantaneous value is given by

$$e(x) = x_Q - x \tag{6}$$

Quantization error can be viewed as an additive signal that distort the input signal.

**Power consideration on system level**

Stability is one of the key factors which influence the actual performance of a DSM. For the single-bit quantizer case, the infinity norm  $\|H\|_\infty$  is traditionally chosen to be 1.5 as rule of thumb to ensure stability [12]. In case of a multibit quantizer  $\|H\|_\infty$  can be increased to improved the signal-to-quantization noise ratio(SQNR).

**Dynamic Range Consideration:**

Software radio implementations typically utilize a wideband front-end, so the dynamic range of the selected

ADC is a very important consideration in a software radio implementation. The Dynamic range in ideal case is given by

$$\text{Dynamic Range}_{ideal} = \text{SQNR} = 6.02 * B + 1.763\text{DB} \quad (7)$$

The Dynamic range(DR) of a practical data converter can be defined as

$$DR_{practical} = 10 \log_{10} \left( \frac{V_{FS}^2 / 12 \eta}{N_Q + N_{Thermal} + \sum_{k=1}^N P_k} \right) \quad (8)$$

Where  $N_{Thermal}$  - Thermal noise and  $P_k$  -power in harmonic.

Dithering is a method that is used to increase spurious free dynamic range[8].

Paper[12] presented one of the first cascaded CT  $\Sigma\Delta$  modulator architecture. The experimental prototype achieved a 77- dB dynamic range, 71-dB peak SNR, and 67-dB peak SNDR over a 7.5MHz signal bandwidth while dissipating 63.6mW of analog power and 89 mW total power[12].

TABLE II PERFORMANCE COMPARISON OF SUB-1-V DSM

Paper	Supply voltage(V)	Process ( $\mu\text{m}$ )	DR (dB)	SNDR (dB)	BW (kHz)	Power ( $\mu\text{W}$ )
[12]	0.9	0.5	77	62	16	40
	0.7	0.18	75	67	8	80
	0.6	0.35	79	78	20	1000
	0.9	0.18	83	80	10	200
	0.5	0.18	76	74	25	300
	0.9	0.13	83	73	20	60

**Thermal Noise**

Thermal noise is the distortion added to a signal from the random movement of electrons in a passive resistive component of the front-end of the ADC. The effects of thermal noise are uncorrelated from sample to sample and can be modeled as a zero mean Gaussian random variable. Thermal noise power is given by the equation

$$P = kTeB \quad (9)$$

Where

K- Bolt Mann’s constant, is  $1.38 * 10^{-23}$  J/k,

Te – the effective temperature of the device in Kelvin,

B – Bandwidth of the input signal.

Software radios have to work with waveform of many different bandwidths, resulting in an operating noise floor that is waveform dependent[3].

**Harmonic Distortion and Spurious Free Dynamic Range**

The analysis of how the harmonics affects the performance of a data converter. This can be simplified by considering the dynamics range effect of only the strongest spurious component within the first Nyquist zone. The dynamics range available in the presence of the SFDR of the data converter and is calculated as

$$\text{SFDR} = 10 \log_{10} \left( \frac{P_o}{\max(P_i)} \right) \text{dB} \quad (10)$$

The main goal is to maximize the SFDR, while minimizing the effect adverse on SNR.

**Signal-to-Noise-and –Distortion Ratio (SINAD)**

Since both noise and distortion degrade signal quality, another commonly used measurement of a data converter’s performance is its signal-to-noise-and distortion (SINAD) ratio. For data converter, the SINAD ratio is defined as the ratio of the signal power,  $P_o$ , to the sum of all the noise sources,  $N$ , plus the distortion from the sum of the harmonics,  $P_i$ , within the first Nyquist zone.

$$\text{SINAD} = 10 \log_{10} \left( \frac{P_o}{N + \sum_{i=1}^{\infty} P_i} \right) \text{dB} \quad (11)$$

**Effective Number of Bits (ENOB)**

Because of distortion and noise, the dynamics range of a practical data converter is less than that of an ideal data converter or is equivalent to an ideal data converter using a lesser number of quantization bits. If either the dynamic range or the SINAD ratio is available, a data converter’s ENOB can be calculated using

$$\text{ENOB} = (\text{SINAD} - 1.763) / 6.02 \quad (12)$$

SINAD ratio (and thus dynamic range) and the ENOB are dependent on frequency and temperature. The number of bits in the ADC defines the upper limit for achievable dynamic range.

**V. CONCLUSION:**

The main requirement of the next generation wireless devices is the support of multiple standards on the same chipset with negligible increase in power consumption. We concluded here that band pass Sigma Delta Analog to Digital converters is better solution in the ideal ADC architecture for software radio application. A brief overview of various parameters of ADC is also discussed in section IV. The section III reviews some of the reported architecture for direct RF digitization and identifies some of their major problem that affects the performance of the ADC.

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